ADC and DAC

1. D/A converters are generally
   a. Weighted resistor network
   b. Binary ladder network
   c. Either (a) or (b)
   d. Neither (a) nor (b)

   Soln. (b)

2. In a 4 bit D/A converter, The offset error is the output voltage when input digital voltage is
   a. 1111
   b. 0000
   c. Either 1111 or 0000
   d. None of the above

   Soln. (b)

3. Which is known as flash converter
   a. Weighted resistor D/A converter
   b. Parallel A/D converter
   c. Stair step A/D converter
   d. Up – down counter type A/D converter

   Soln. (b)

   Flash ADC is the fastest of all D/A converters and uses 2^{n-1} comparators. It is expansive

4. Which converters uses integrating op-amp
   a. Parallel A/D converter
   b. Single slope A/D converter
   c. Dual slop A/D converter
   d. Both (b) and (c)

   Soln. (c)

   The core of the dual slope A/D converter is the integrating op-amp and thus it has good noise immunity and its accuracy is high. It requires 2.2^n twice the ramp type clock cycles for conversion.

5. The accuracy of A/D conversion is generally

a. $\pm\frac{1}{2}\ LSB$
b. $\pm\ LSB$
c. $\pm\ \frac{5}{4}\ LSB$
d. None of the above

Soln. (a)

It is half of the resolution of A/D converter

6. The number of counter states which an 8 bit stair step A/D converter has to pass through before conversion is

a. 1
b. 8
c. 255
d. 256

Soln. (d)

The number of counter states for 8 bit ramp type A/D converter is $2^8 = 256$

7. An n bit ADC using V as reference has a resolution of

a. $\frac{V}{2^n}$
b. $V(n)$
c. $\frac{V}{2^n-1}$
d. 2 V (n)

Soln. (c)

Each successive binary count is equal to $\frac{1}{2^n-1}$ of the total, so the resolution of n bit ADC using V as reference is $\frac{V}{2^n-1}$

8. A 6 bit ladder D/A converter has input 101001. For 1 = 10 V and 0 = 0V, The output is

a. 4.23
b. 6.51
c. 5.52
d. 9.23

Soln. (b)

For a 6 bit D/A converter whose output varies from 0 to 10V, the resolution is

$$\boldsymbol{Res = \frac{10}{2^6 - 1} = \frac{10}{63} = 0.1587}$$

The resolution is the smallest analog change in the output or a change in one LSB

So $101001 = (41)_{10}$

So output is $41 \times 0.1587 = 6.51V$

9. A 10 bit D/A converter given a maximum output of 10.23V. The resolution is
   a. 10 mV
   b. 20 mV
   c. 15 mV
   d. 25 mV

   Soln. (a)

   Resolution $\frac{10.23}{2^{10}-1} = \frac{10.23}{1023} = \frac{1}{100}\ volts = 10mv$

10.
   a. Successive approximation
   b. Dual slope
   c. Parallel comparator

   Maximum conversion time for 8 bit ADC in clock cycles
   (1) 1
   (2) 8
   (3) 16
   (4) 256
   (5) 512

   Soln. Options a – 2, b – 5, c – 1,

   For n bit ADC, the conversion time for

   a. Successive approximation $= n\ clock\ cycles = 8\ T_{CK}$
   b. Dual slope= $2\ 2^n T_{CK} = 2^{n+1} T_{CK} = 512\ T_{CK}$
   c. Parallel comparator: $1\ clock\ cyclye = 1T_{CK}$

11. For an ADC, match the following : if

   List – I
   (a) Flash converter
   (b) Dual slope converter
   (c) Successive approximation converter

   List – II

(1) Requires a conversion time of the order of a few seconds
(2) Requires a digital-to-analog converter
(3) Minimizes the effect of power supply interference.
(4) Requires a very complex hardware
(5) Is a tracking A/D converter.

[GATE 1995 : 1 Mark]

Soln. Flash converter or parallel A/D converter is fastest of all but requires a complex hardware. Dual slope integrator has good noise immunity and thus minimizes the effect of power supply interference. Successive approximation has shorter conversion time of the order of μsec and depends upon the number of bits only. For n bit ADC, it requires n clock cycles. It uses D/A converter.

A – 4, B – 3, C – 2

12. The advantage of using a dual slope ADC in a digital voltmeter is that
    a. Its conversion time is small
    b. Its accuracy is high
    c. It gives output in BCD format
    d. It does not require a comparator

[GATE 1998 : 1 Mark]

Soln. (b)

13. An 8 bit successive approximation analog to digital converter has full scale reading of 2.55 V and its conversion time for an analog input of 1V is 20μs. The conversion time for a 2V input will be
    a. 10 μs
    b. 20 μs
    c. 40 μs
    d. 50 μs

[GATE 2000 : 1 Mark]

Soln. (b)

The conversion time of successive approximate ADC depends upon the number of bitsonly.

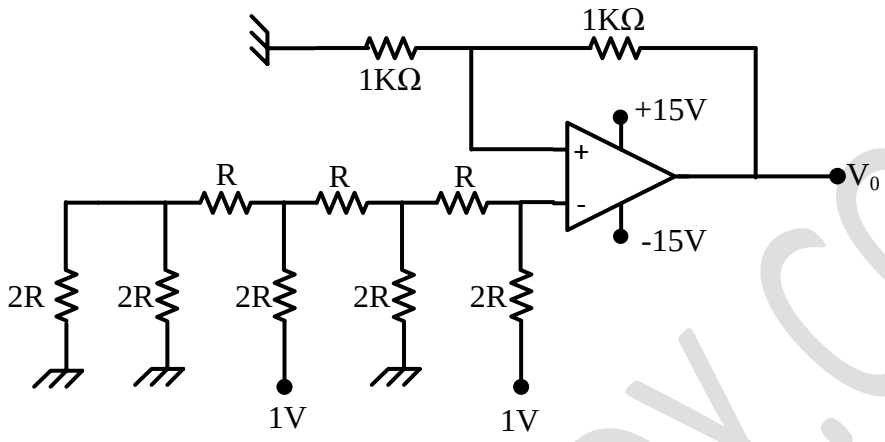
14. The number of comparators in a 4-bit flash ADC is
    a. 4
    b. 5
    c. 15
    d. 16

[GATE 2000 : 1 Mark]

Soln. (c)

The number of comparators in a flash ADC is equal to $2^n - 1 = 2^4 - 1 = 15$

15. For the 4 bit DAC shown in the figure, the output voltage V_0 is



a. 10 V
b. 5 V
c. 4 V
d. 8 V

[GATE 2000 : 2 Marks]

Soln. (b)

V_{in} at the non inverting terminal $= \frac{1}{8} + \frac{1}{2} = \frac{5}{8}$

$$V_0 = \left(1 + \frac{R_f}{R}\right) V_{in} = 8 \times \frac{5}{8} = 5V$$

16. A digital system is required to amplify a binary encoded audio signal. The user should be able to control the gain of the amplifier from a minimum to a maximum in 100 increments. The minimum number of bits required to encode, in straight binary, is

a. 8
b. 6
c. 5
d. 7

[GATE 2004 : 1 Mark]

Soln. (d)

$$2^n > 100$$

$$n \geq 7$$