Digital Integrated Circuits - Logic Families (Part II)

MOSFET Logic Circuits

- MOSFETs are unipolar devices. They are simple, small in size, inexpensive to fabricate and consume less power.
- MOS fabrication is simpler than TTL and greater packing density
- JFETs for linear circuits & MOSFETs for digital circuits.
- Fabricated in less area than BJT
  Two types of MOS structure,
  (i) N MOS – Majority carriers electrons
  (ii) P MOS – Majority carriers Holes
- Depletion type or enhancement type
- MOS devices can be used as transistor as well as resistor
- P MOS & N MOS digital ICs have greater packing density than CMOS
- N MOS will be twice as fast as P MOS
- N MOS & P MOS find applications in LSIs like μPs, memories etc.
CMOS for MSI applications.
The circuits for N MOS inverter and N MOS NAND are given

Q<sub>2</sub> – Depletion Mode MOSFET
\[ V_{GS2} = 0 \text{ V, } Q_2 \text{ – ON} \]
Behaves as Resistor
Q<sub>1</sub> – Enhancement MOS
\[ V_{in} \text{ +ve it conducts, LOW} \]
\[ V_{in} \text{ 0V it turns off, HIGH} \]

N MOS Inverter – Active Pull up
$Q_1$ & $Q_2$ are enhancement mode switching transistor

$Q_3$ is depletion mode pull up as active load

Logic 1 turns on respective transistor

Logic 0 turns off respective transistor

Both transistor on to generate logic 0 at output

Either or both off output at logic 1

Thus behaves as NAND GATE
Complementary MOS Logic (CMOS):

- Complementary Symmetry Metal Oxide Semiconductors COSMOS or CMOS. They are made using PMOS and NMOS.
- CMOS make use of both N MOS & P MOS.
- Power consumption under static condition is extremely low.
- CMOS excel PMOS and NMOS due to:
  (i) Low power dissipation
  (ii) Enhanced noise immunity
  (iii) High fan out and
  (iv) Ease of interfacing
- CMOS fabrication is simpler than TTL and greater packing density.
- CMOS captured the market due to its very low power and competitive speed.
C MOS inverter, NAND & NOR circuits are given

- C MOS make use of both N MOS & P MOS
- N MOS & P MOS complementary devices
- Both $Q_1$ & $Q_2$ are enhancement type
- When $V_{in} = 0$ V $Q_1$ cut off (N MOS needs $+V_{GS}$)
  $V_{GS2} = -V_{DD}$, $Q_2$ is ON
  output $V_{DD}$
• Two N MOS transistors at the bottom in series.
• Two P MOS on top are connected in parallel
• Form two pairs – each with N & P MOSFETs
• Let \( V_A = V_B = 0 \) \( Q_3 \) and \( Q_4 \) cutoff. \( Q_1 \) & \( Q_2 \) conducting. Output at logic 1
• Let \( V_A = 0 \) & \( V_B = 1 \), \( Q_3 \) cutoff & \( Q_4 \) conducting, \( Q_1 \) is ON & \( Q_2 \) is off. (one transistor on provides direct connection between \( V_{DD} \) & \( V_{out} \)). \( V_{out} = 1 \)
• Similarly, for \( V_A = 1 \) & \( V_B = 0 \)
  \( V_A = V_B = 1 \), Both \( Q_3 \) & \( Q_4 \) conducting & \( Q_1 \) and \( Q_2 \) off.
  \( V_{out} = 0 \)
• 2 input CMOS NOR
• Switching transistors Q₁ and Q₂ connected in parallel
• If both transistors ON the output is logic 0
• Both Q₁ and Q₂ OFF to generate logic 1 at output
MOS LOGIC – Sub FAMILIES

- First C MOS family 4000 series by RCA works with 15 V supply
- C MOS sub families
  - HC - (High Speed)
  - HCT - (High Speed TTL Compatible)
  - AC - (Advanced C MOS)
  - ACT - (Advanced TTL compatible)

C MOS Sub Families Characteristics

<table>
<thead>
<tr>
<th>Family</th>
<th>74 HC</th>
<th>74 HCT</th>
<th>74 AC</th>
<th>74 ACT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{\textsubscript{CC}}</td>
<td>5 V</td>
<td>5 V</td>
<td>5 V</td>
<td>5 V</td>
</tr>
<tr>
<td>t\text{\textsubscript{pd}} (ns)</td>
<td>18</td>
<td>18</td>
<td>11.1</td>
<td>12.3</td>
</tr>
<tr>
<td>Pd (\mu W)</td>
<td>2.5</td>
<td>2.5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>(Steady State Speed Power Product (pJ)</td>
<td></td>
<td></td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>100 KHz</td>
<td>1.1</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
• AC/ACT Best speed power product.
• 74 AHC/AHCT (Advanced high speed C MOS these are advanced versions, so faster)

C MOS Logic

• Best suited for battery operated circuits.
• In high noise environment C MOS is better suited than TTL
• Unused C MOS input should be left open
• C MOS switching speed decreases with operating frequency.
• C MOS switching speed increase with supply voltage
• C MOS fan out is determined by
  (i) Maximum permissible propagation delay
  (ii) Input capacitance of each load

Low voltage Technology

Efforts have been increase chip density for

  o More circuits on the chip
  o Increasing operating speed (due to proximity)

But it increase chip dissipation.

Allowing chips at lower voltage power dissipation can be reduced.
Typical voltages are 3.3 V, 2.5 V etc.

Newer CPUs are 2.5 V devices & 3.3 V dynamic RAM in memory modules of PCs.

### Comparison of Logic Families

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>TTL</th>
<th>ECL</th>
<th>MOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Std.</td>
<td>74 AS</td>
<td>74 ALS</td>
<td>1000</td>
</tr>
<tr>
<td>Fan out</td>
<td>10</td>
<td>40</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>Power dissipation (mW)</td>
<td>10</td>
<td>10</td>
<td>1</td>
<td>50</td>
</tr>
<tr>
<td>Noise Immunity</td>
<td>Very good</td>
<td>Very good</td>
<td>Very good</td>
<td>Poor</td>
</tr>
<tr>
<td>Prop. delay (ns)</td>
<td>10</td>
<td>1.5</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Speed power product (pJ)</td>
<td>100</td>
<td>15</td>
<td>4</td>
<td>100</td>
</tr>
</tbody>
</table>

**Observations:**

- TTL series best at high frequency is 74 AS
- TTL series best for battery operated circuits is 74 ALS
- ECL is the fastest logic family (unsaturated)
• Best speed - power product (or FOM ) is 74 ACT (for battery operated circuits)
## High Speed Logic Comparisons (Newer Series)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>TTL</th>
<th>C MOS</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>74 AS</td>
<td>74 F</td>
<td>74 AHC</td>
</tr>
<tr>
<td><strong>T&lt;sub&gt;pd&lt;/sub&gt; (ns)</strong></td>
<td>1.7</td>
<td>3.8</td>
<td>3.7</td>
</tr>
<tr>
<td><strong>P&lt;sub&gt;D&lt;/sub&gt; (mW)</strong></td>
<td>8</td>
<td>6</td>
<td>0.006</td>
</tr>
<tr>
<td><strong>Noise Margin (mV)</strong></td>
<td>300</td>
<td>300</td>
<td>550</td>
</tr>
<tr>
<td><strong>Speed power product (p-J)</strong></td>
<td>13.6</td>
<td>22.8</td>
<td>0.02</td>
</tr>
</tbody>
</table>

CML – Current mode logic  
74 ALB – Advanced low voltage Bi C MOS  
74 AHC – Advanced high speed C MOS  
74 AVC – Advanced very low voltage C MOS (2.5 V)  
   (Propagation delay of 2 ns rivals 74 AS bipolar)