Digital Integrated Circuits - Logic Families (Part II)

MOSFET Logic Circuits

- MOSFETs are unipolar devices. They are simple, small in size, inexpensive to fabricate and consume less power.
- MOS fabrication is simpler than TTL and greater packing density
- JFETs for linear circuits & MOSFETs for digital circuits.
- Fabricated in less area than BJT
  Two types of MOS structure,
  (i) N MOS – Majority carriers electrons
  (ii) P MOS – Majority carriers Holes
- Depletion type or enhancement type
- MOS devices can be used as transistor as well as resistor
- P MOS & N MOS digital ICs have greater packing density than C MOS
- N MOS will be twice as fast as P MOS
- N MOS & P MOS find applications in LSIs like µPs, memories etc.

- CMOS for MSI applications.
  The circuits for N MOS inverter and N MOS NAND are given

Q_2 – Depletion Mode MOSFET

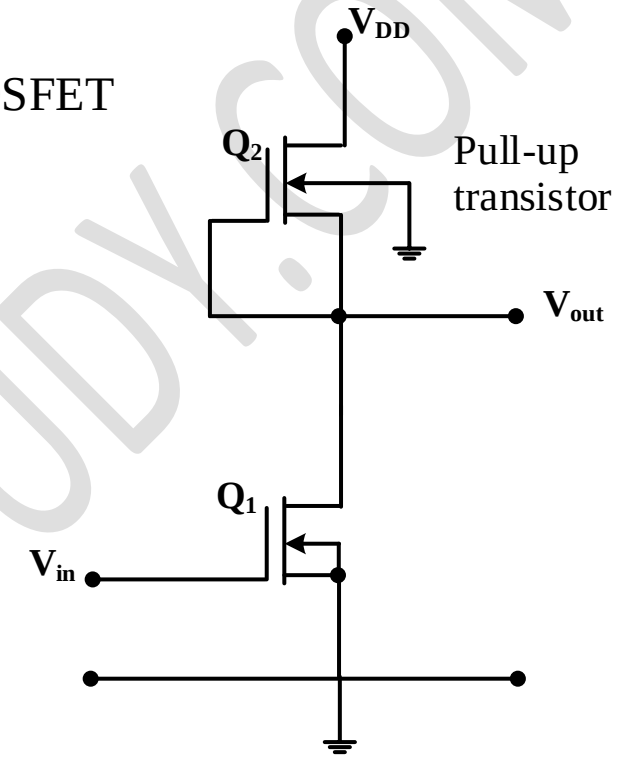
V_{GS2} = 0 V, Q_2 – ON

Behaves as Resistor

Q_1 – Enhancement MOS

V_{in} +ve it conducts ,LOW

V_{in} 0V it turns off ,HIGH



N MOS Invertor – Active Pull up

Q_1 & Q_2 are enhancement mode switching transistor

Q_3 is depletion mode pull up as active load

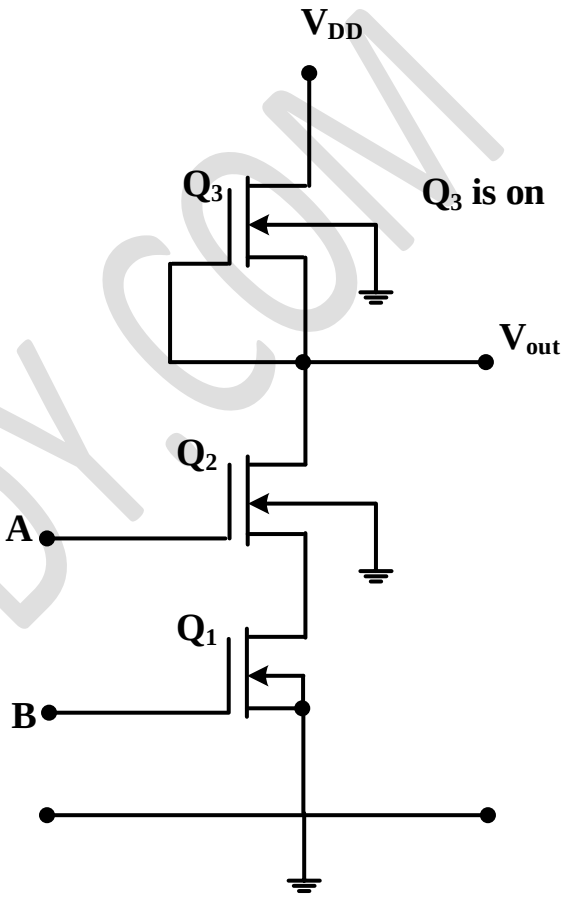
Logic 1 turns on respective transistor

Logic 0 turns off respective transistor

Both transistor on to generate logic 0 at output

Either or both off output at logic 1

Thus behaves as NAND GATE



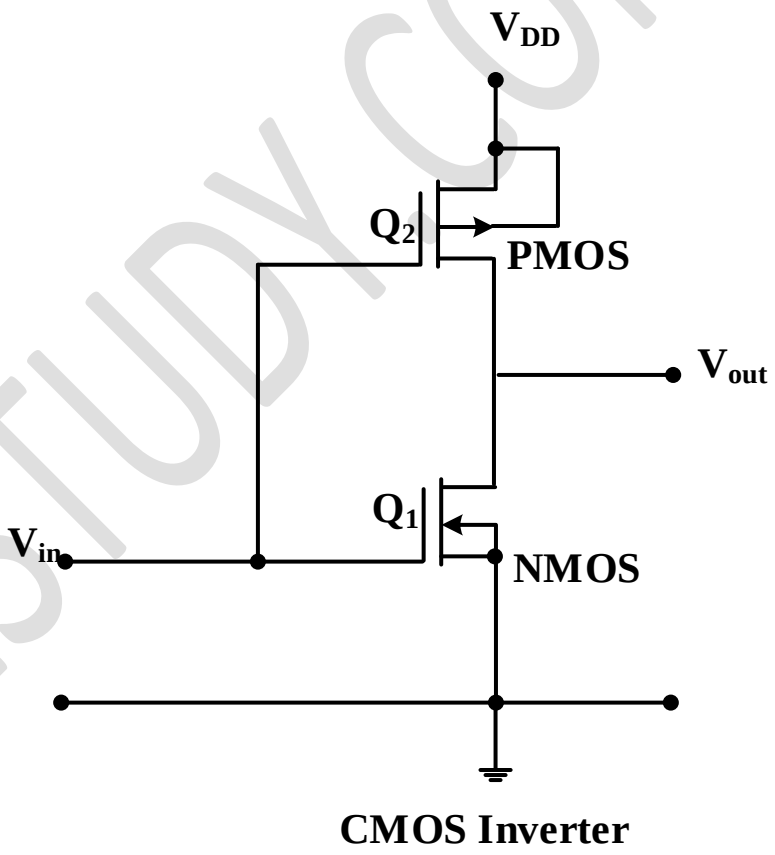
N MOS NAND GATE

Complementary MOS Logic (CMOS):

- Complementary Symmetry Metal Oxide Semiconductors COSMOS or CMOS .They are made using PMOS and NMOS
- C MOS make use of both N MOS & P MOS
- Power consumption under static condition is extremely low.
- CMOS excel PMOS And NMOS due to
  (i) Low power dissipation
  (ii) Enhanced noise immunity
  (iii) High fan out and
  (iv) Ease of interfacing
- CMOS fabrication is simpler than TTL and greater packing density.
- C MOS captured the market due to its very low power and competitive speed.

C MOS inverter, NAND & NOR circuits are given

- C MOS make use of both N MOS & P MOS
- N MOS & P MOS complementary devices
- Both Q_1 & Q_2 are enhancement type
- When $V_{in} = 0$ V Q_1 cut off (N MOS needs $+V_{GS}$) $V_{GS2} = -V_{DD}$, Q_2 is ON output V_{DD}

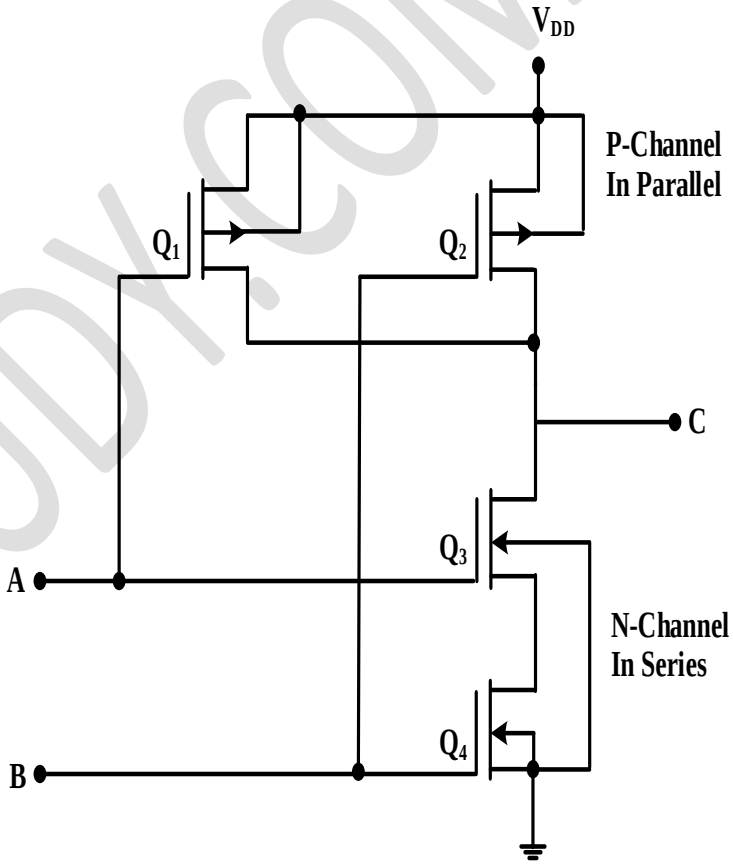


CMOS Inverter

- Two N MOS transistors at the bottom in series.
- Two P MOS on top are connected in parallel
- Form two pairs – each with N & P MOSFETs
- Let $V_A = V_B = 0$ Q_3 and Q_4 cutoff. Q_1 & Q_2 conducting. Output at logic 1
- Let $V_A = 0$ & $V_B = 1$, Q_3 cutoff & Q_4 conducting, Q_1 is ON & Q_2 is off. (one transistor on provides direct connection between V_{DD} & V_{out}). $V_{out} = 1$
- Similarly, for $V_A = 1$ & $V_B = 0$

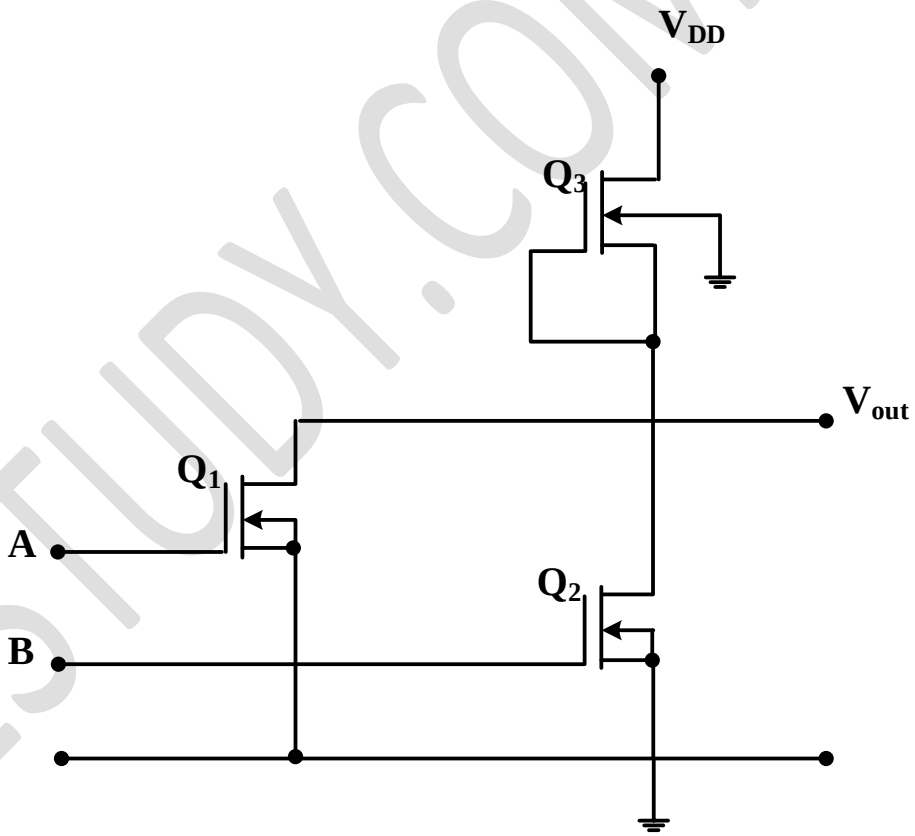
$V_A = V_B = 1$, Both Q_3 & Q_4 conducting & Q1 and Q_2 off.

$V_{out} = 0$



Two-input CMOS NAND

- 2 input CMOS NOR
- Switching transistors Q_1 and Q_2 connected in parallel
- If both transistors ON the output is logic 0
- Both Q_1 and Q_2 OFF to generate logic 1 at output



MOS LOGIC – Sub FAMILIES

- First C MOS family 4000 series by RCA works with 15 V supply
- C MOS sub families

  HC - (High Speed)
  HCT - (High Speed TTL Compatible)
  AC - (Advanced C MOS)
  ACT - (Advanced TTL compatible)

C MOS Sub Families Characteristics

Family	74 HC	74 HCT	74 AC	74 ACT
V_{CC}	5 V	5 V	5 V	5 V
t_{pd} (ns)	18	18	11.1	12.3
Pd (μW) (Steady State	2.5	2.5	5	5
Speed Power Product (pJ) 100 KHz	1.1	1.1	0.4	0.4

- AC/ACT Best speed power product.
- 74 AHC/AHCT (Advanced high speed C MOS these are advanced versions, so faster)

C MOS Logic

- **Best suited for battery operated circuits.**
- **In high noise environment C MOS is better suited than TTL**
- **Unused C MOS input should be left open**
- **C MOS switching speed decreases with operating frequency.**
- **C MOS switching speed increase with supply voltage**
- **C MOS fan out is determined by**
  (i) Maximum permissible propagation delay
  (ii) Input capacitance of each load

Low voltage Technology

Efforts have been increase chip density for

- **More circuits on the chip**
- **Increasing operating speed (due to proximity)**

But it increase chip dissipation.

Allowing chips at lower voltage power dissipation can be reduced.

Typical voltages are 3.3 V, 2.5 V etc.

Newer CPUS are 2.5 V devices & 3.3 V dynamic RAM in memory modules of PCs.

Comparison of Logic Families

Characteristics	**TTL**			**ECL**	**MOS**	**CMOS**	
	Std.	74 AS	74 ALS	1000		74 C	74 ACT
Fan out	10	40	20	25	20	50	50
Power dissipation (mW)	10	10	1	50	0.5	0.01	0.005
Noise Immunity	Very good	Very good	Very good	Poor	Good	Excellent	Excellent
Prop. delay (ns)	10	1.5	1	2	300	70	4.75
Speed power product (pJ)	100	15	4	100	60	70	0.5

Observations:

- TTL series best at high frequency is 74 AS
- TTL series best for battery operated circuits is 74 ALS
- ECL is the fastest logic family (unsaturated)

- Best speed - power product (or FOM) is 74 ACT (for battery operated circuits)

High Speed Logic Comparisons (Newer Series)

Characteristics	TTL		C MOS			CML
	74 AS	74 F	74 AHC	74 AVC	74 ALB	ECL
T_{pd} (ns)	1.7	3.8	3.7	2	2.2	0.3
P_D (mW)	8	6	0.006	0.006	1	25
Noise Margin (mV)	300	300	550	250 mV	400	150
Speed power product (p-J)	13.6	22.8	0.02	0.012	2.2	7.5

CML – Current mode logic

74 ALB – Advanced low voltage Bi C MOS

74 AHC – Advanced high speed C MOS

74 AVC – Advanced very low voltage C MOS (2.5 V)

(Propagation delay of 2 ns rivals 74 AS bipolar)