# P N Junction Theory and diodes (Part I) – GATE Problems

1. In a junction diode
   (a) the depletion capacitance increases with increase in the reverse bias
   (b) the depletion capacitance decreases with increase in the reverse bias
   (c) the depletion capacitance increases with increase in the forward bias
   (d) the depletion capacitance is much higher than the depletion capacitance when it is forward biased

**[GATE 1990: 1 Mark]**

**Soln. Depletion capacitance has other names such as space charge capacitance, transition capacitance or barrier capacitance. This capacitance occurs when the junction is reverse biased. Junction behaves as a parallel plate capacitance whose capacitance is given by**

$$C_T = \frac{\in A}{W}$$

**Where, A – cross section area of junction**

**W – Thickness of space charge**

$\in$ **- Dielectric constant**

**Thus when reverse bias increases, depletion layer width** $(W)$ **increases, so capacitance decreases as per above equation**

**Option (b)**

2. The diffusion potential across a p n-junction
   (a) decreases with increasing doping concentration
   (b) increases with decreasing band gap
   (c) does not depend on doping concentrations
   (d) increases with increases in doping concentration

**[GATE 1995: 1 Mark]**

**Soln. The term diffusion potential also has other names such that Barrier potential, Built in potential, and contact potential.**

**Diffusion potential or built in potential across the P – N junction is given by**

$$V_{bi} = \frac{kT}{q} ln\left(\frac{N_A N_D}{n_i^2}\right)$$

**Where,**

**$N_D$ – Donor concertation on n – side**

**$N_A$ – Acceptor concentration on p – side**

**If temperature is constant and $n_i$ (intrinsic concentration) is constant**

**Diffusion potential $\propto \ln(N_A N_D)$**

**So, option (d)**

3. A Zener diode works on the principle of
   (a) tunnelling of charge carriers across the junction
   (b) thermionic emission
   (c) diffusion of charge carriers across the junction
   (d) hopping of charge carriers across the junction

**[GATE 1995: 1 Mark]**

**Soln. Zener diode has heavily doped p – n junction. It operates under the reverse bias.**

**When heavily doped junction is reverse biased energy bands become crossed at relatively low voltages i.e. n side conduction band appears opposite to p – side valence band. Crossing of bands allows large number of empty states is n side conduction band opposite to many filled states of the p – side valence band. If barrier is narrow, tunnelling of electrons can occur.**

**Tunnelling of electrons from p – side valence band to n – side conduction band constitutes a reverse current from n to p this is Zener effect**

**Thus, option (a)**

4. The depletion capacitance, $C_j$ of an abrupt p – n junction with constant doping on either side varies with Reverse Bias $V_R$ as
   (a) $C_J \propto V_R$
   (b) $C_J \propto V_R^{-1}$
   (c) $C_J \propto V_R^{-1/2}$
   (d) $C_J \propto V_R^{-1/3}$

**[GATE 1995: 1 Mark]**

**Soln. When p – n junction is formed a depletion layer is formed on either side of the junction. It acts like a dielectric (non- conductive) between p and n regions.**

**P and N regions have low resistance, so they act like two plates of a capacitor. Thus capacitance is formed which has different names like depletion region capacitance, space charge capacitance, transition capacitance or junction capacitance. This capacitance is related as**

$$C_J = \frac{K}{(V_B - V_R)^n} \cong \frac{K}{V_R^n}$$

**Where,**

**K – Constant that depends on nature of semiconductor material,**

**$V_D$ – Barrier voltage**

$$for \;\; S_i \;\; , \quad V_B = 0.7\,V$$

$$G_e \;\; , \quad V_B = 0.3\,V$$

**$V_R$ – Applied reverse bias**

**n – 1/2 for step junction**

**1/3 for linearly graded junction**

**Since the given problem is of abrupt junction**

**So, n = 1/2**

**Option (c)**

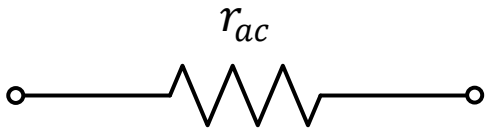
5. For small signal ac operation, a practical forward biased diode can be modelled as
(a) a resistance and a capacitance
(b) an ideal diode and resistance in parallel
(c) a resistance and an ideal diode in series
(d) a resistance

**[GATE 1998: 1 Mark]**

**Soln. For small signal ac operation the practical forward biased diode can be modelled as a resistance $(r_{ac})$ given by the reciprocal of the slope of the characterises at that point**

$$r_{ac} = \frac{1}{\Delta I_F / \Delta V_F} = \frac{\Delta V_F}{\Delta I_F}$$

**Its equivalent circuit is given as**




**Option (d)**

6. The static characteristic of an adequately forward biases p-n junction is a straight line, if the plot is of
   (a) log I vs log V
   (b) log I vs V
   (c) I vs log V
   (d) I vs V

**[GATE 1998: 1 Mark]**

**Soln. Diode equation is given by**

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

**Where,**

**V – Diode voltage**

**$V_T$ – Volt equivalent of temp.( = $kT/q$)**

**$\eta$ – A constant**

**= 1 for Ge diode**

**= 2 for Si diode**

**(For diode current below knee voltage)**

**$\eta$ = 1 for Ge and Si for large currents.**

**For adequately forward biased p – n junction**

$$e^{V/\eta V_T} \gg 1$$

**Or,**

$$I = I_0 \, e^{V/\eta V_T}$$

**Or,**

$$\frac{V}{\eta V_T} = \ln\left(\frac{I}{I_0}\right)$$

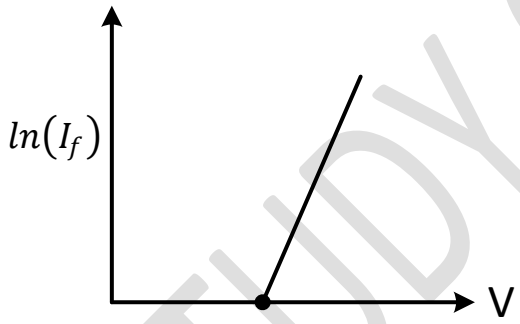
$$V = \eta V_T \ln(I) - \eta V_T \ln(I_0)$$

**Compare with standard curve**

$$y = mx + c$$

$$m = \eta V_T \quad , \quad x = \ln(I)$$

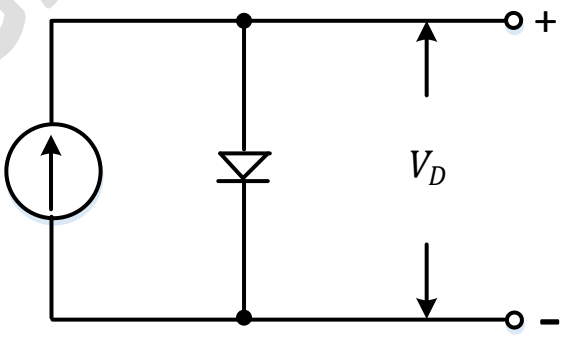
**and** $c = -\eta \, V_T \ln(I_0)$




**Thus the plot is straight line.**

**Option (b)**

7. In the figure, silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20℃, $V_D$ is found to be 700 mV. If the temperature rises to 40℃, $V_D$ becomes approximately equal to



(a) 740 mV
(b) 660 mV
(c) 680 mV
(d) 700 mV

**[GATE 2002: 1 Mark]**

**Soln. In the given figure**

**Diode is Silicon diode carrying forward current of 1mA.**

**Diode voltage is 700 mV at $20℃$. We have to find forward diode voltage when temperature is $40℃$. Note that diode equation is**

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

**Where,** $V_T = \frac{kT}{q} = \frac{T}{11{,}600}$

**Thus when temperature increases the exponential term will decrease thus reducing the diode current. This reduction in voltage is found to be (for $G_e$ or $S_i$)**

$$\frac{dV}{dT} \cong -2m\ V/℃$$

**Thus for $20℃$ increase in temperature i.e. $(T_2 - T_1) = 20℃$ voltage will be $-2 \times 20 = -40mv$**

**Thus, $V_D = 700 - 40 = 660mV$**

**Option (b)**

8. Choose proper substitutes for X and Y to make the following statement correct. Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively.
(a) X: reverse, Y: reverse
(b) X: reverse, Y: forward
(c) X: forward, Y: reverse
(d) X: forward, Y: forward

**[GATE 2003: 1 Mark]**

**Soln. Note, that Tunnel diodes operate in forward bias giving negative resistance region while Avalanche photo diodes (APDs) operate at high reverse bias**

**Thus Option (c)**

9. A Silicon PN junction at temperature of 20℃ has a reverse saturation current of 10 pico-Amperes (pA). The reverse saturation current at 40℃ for the same bias is approximately

(a) 30 pA
(b) 40 pA
(c) 50 pA
(d) 60 pA

**[GATE 2005: 1 Mark]**

**Soln. The variation of reverse saturation current is much larger than the exponential term.**

**The reverse saturation current doubles for every 10℃ increase in temperature**

**It can be expressed as**

$$I_{0_2} = I_{0_1} . 2^{(T_2 - T_1)/10}$$

**For $G_e$ and $S_i$**

**So,**

$$I_{0_2} = 10 \times 2^{(40-20)/10}$$

$$= 10 \times 2^2$$

$$I_{0_2} = 40\ pA$$

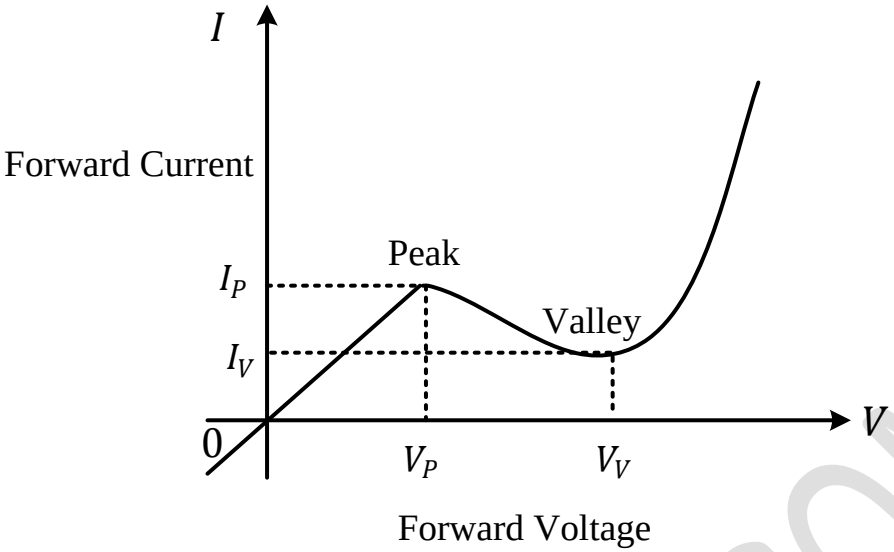
**Option (b)**

10. The values of voltage ($V_D$) across a tunnel-diode corresponding to peak and valley currents are $V_p$ and $V_v$ respectively. The range of tunnel-diode voltage $V_D$ for which the slope of its I – $V_D$ characteristics is negative would be

(a) $V_D < 0$
(b) $0 \leq V_D < V_P$
(c) $V_P \leq V_D < V_V$
(d) $V_D \geq V_V$

**[GATE 2006: 1 Mark]**

**Soln. Current voltage characteristics of tunnel diode is shown below**




**Where,**

**$V_D$ – Voltage across Tunnel diode**

**$V_P$ – Peak value current**

**$V_V$ – Valley value current**

**Range of tunnel diode voltage for which the slope of the characteristics is –ve is between $V_P$ and $V_V$**

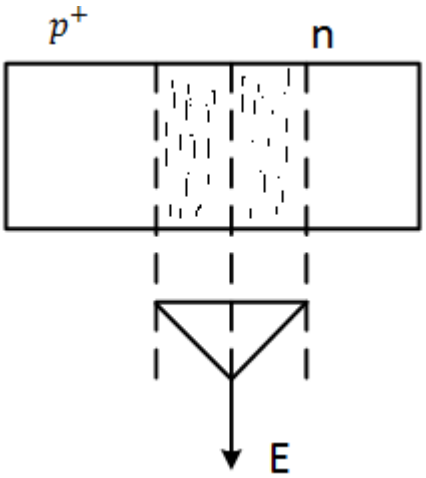
**Option (c)**

11. In a $p^+n$ junction diode under reverse bias, the magnitude of electric field is maximum at
(a) the edge of the depletion region on the p-side
(b) the edge of the depletion region on the n-side
(c) the $p^+n$ junction
(d) the centre of the depletion region on the n-side

**[GATE 2007: 1 Mark]**

**Soln. Given,**

**The junction is $p^+n$ type i.e. p region is highly doped and n region is lightly doped**




**Depletion region is narrow towards p+ side than n side. The electric filed is maximum at the junction point**

**Option (c)**

12. Which of the following is NOT associated with a p-n junction?
    (a) Junction Capacitance
    (b) Charge Storage Capacitance
    (c) Depletion Capacitance
    (d) Channel Length Modulation

**[GATE 2008: 1 Mark]**

**Soln. The terms,**

**(a) Junction capacitance, Charge storage and Depletion capacitance are related to p – n junction but option (d) Channel length modulation is not related to p – n junction.**
**Thus , option(d)**

13. A Silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10℃, the forward bias voltage across the PN junction
    (a) increases by 60 mV
    (b) decreases by 60 mV
    (c) increases by 25 mV
    (d) decreases by 25 mV

**[GATE 2011: 1 Mark]**

**Soln. For the forward biased P – N junction, as the temperature increases the forward voltage decreases by $2.5mV/℃$ which can be written**

**as**

$$\frac{dV}{dT} = -2.5mv/℃$$

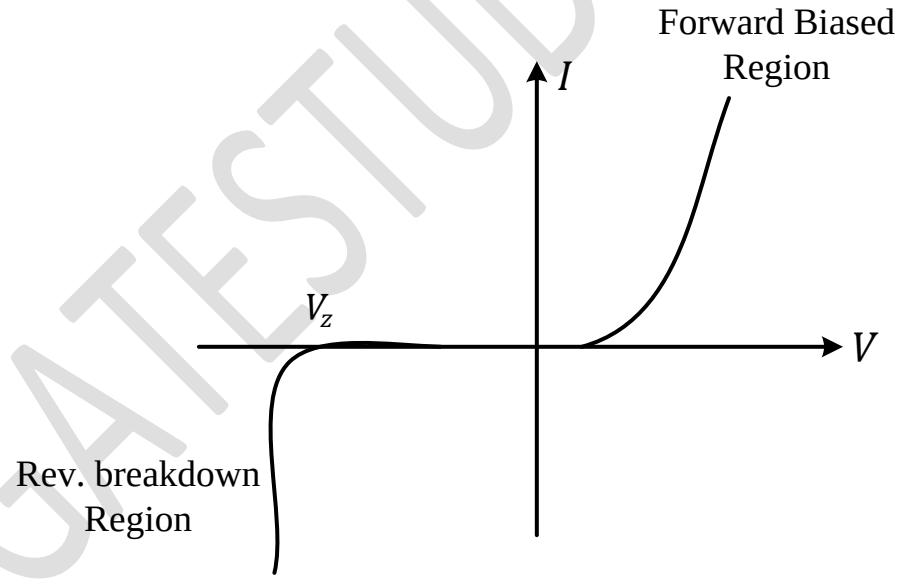
**For 10℃ increase the voltage will be $-2.5 \times 10 = -25mv$**

**So, Option (d)**

14. A Zener diode, when used in voltage stabilization circuits, is biased in
(a) reverse bias region below the breakdown voltage
(b) reverse breakdown region
(c) forward bias region
(d) forward bias constant current mode

**[GATE 2011: 1 Mark]**

**Soln. When Zener diode is forward biased, it behaves as normal diode. Zener diode is operated in its reverse biased breakdown region, when the voltage across the device remains constant as the reverse current varies over a large range.**

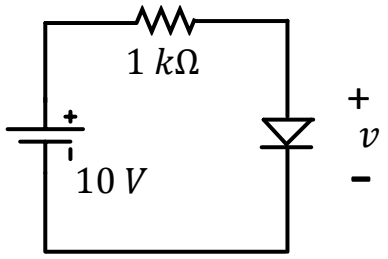



**This is used as voltage reference in stabilisation circuits. Figure shows the characteristics.**

**Option (b)**

15. The I – V characteristics of the diode in the circuit given below are

$$i = \begin{cases} \dfrac{v - 0.7}{500} A, & v \geq 0.7V \\ 0\ A, & v < 0.7V \end{cases}$$

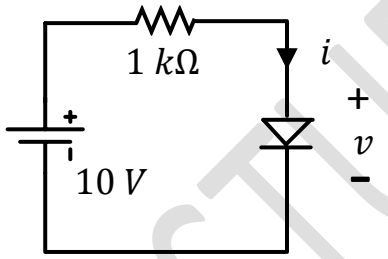



The current in the circuit is

(a) 10 mA
(b) 9.3 mA
(c) 6.67 mA
(d) 6.2 mA

**[GATE 2012: 1 Mark]**

**Soln. Let I be the current flowing through the circuit.**




**applying KVL**

$$\mathbf{10 - 1000\, i - v = 0} \quad - \quad (\boldsymbol{i})$$

**The voltage applied is 10V, so the diode is forward biased and forward current will flow through the diode as given**

$$\boldsymbol{i = \frac{v - .07}{500} A \quad for\ v < 0.7\ V} \quad - \quad (\boldsymbol{ii})$$

**Substituting for i equation (i)**

$$\mathbf{10 - 1000 \times \frac{(v - 0.7)}{500} - v = 0}$$

$$\boldsymbol{or}, \quad \mathbf{10 - 2(v - 0.7) - v = 0}$$

$$\boldsymbol{or}, \quad \mathbf{3v = 11.4}$$

$$or, \quad v = 3.8V$$

$$or, \quad i = \frac{v - 0.7}{500} = \frac{3.8 - 0.7}{500}$$

$$= 6.2mA$$

**Option (d)**

16. In a forward biased p - n junction, the sequence of events that best describes the mechanism of current flow is
    (a) injection, and subsequent diffusion and recombination of minority carriers
    (b) injection, and subsequent drift and generation of minority carriers
    (c) extraction of subsequent diffusion and generation of minority carriers
    (d) extraction, and subsequent drift and recombination of minority carriers

**[GATE 2013: 1 Mark]**

**Soln. In a forward biased p – n junction diode the current flow is due to**

**(i) diffusion of majority carries**

**(ii) recombination of minority carriers**

**However, injection has to precede the sequence of above operations.**

**Thus , Option (a)**

17. When the optical power incident on a photodiode is 10 µW and the responsivity is 80 A/W, the photocurrent generated (in µA) is _____

**[GATE 2014: 1 Mark]**

**Soln. Responsivity of the photo diode is defined as**

$$Responsivity \ (R) = \frac{I_P}{P_{op}}$$

**Where $I_P$ – is generated photo current**

**And $P_{op}$ – Incident optical power**

$$\mathcal{R} = \frac{I_P}{P_0}$$

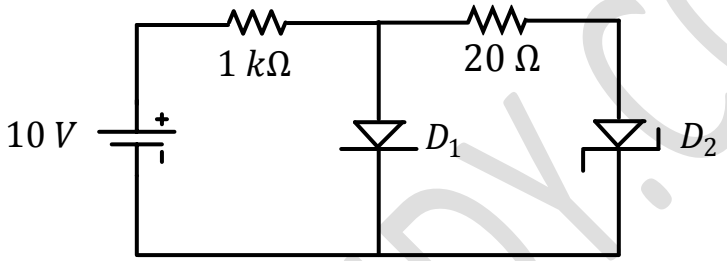
$$or,\ I_P = \mathcal{R} \times P_0$$

$$= 0.8 \times 10 \times 10^{-6}$$

$$= 8\mu A$$

**Ans.** $8\mu A$

18. In the figure assume that the forward voltage drops of the PN diode $D_1$ and Schottky diode $D_2$ are 0.7 and 0.3 V, respectively. If ON OFF denotes non-conducting state of the diode, then in the circuit




(a) both $D_1$ and $D_2$ are ON
(b) $D_1$ is ON and $D_2$ is OFF
(c) both $D_1$ and $D_2$ are OFF
(d) $D_1$ is OFF and $D_2$ is ON

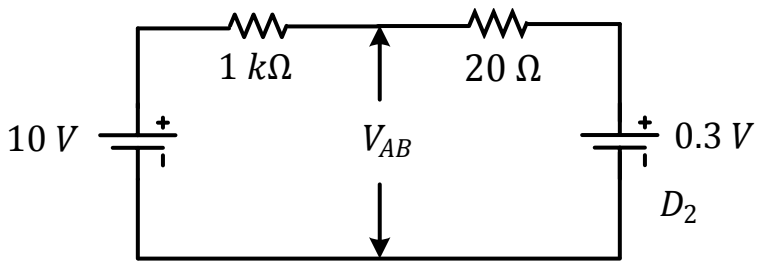
**[GATE 2014: 1 Mark]**

**Soln. In the given figure the cut voltage of $D_2$ is less than $D_1$, so it should start conducting earlier.**

**Thus we assume**

**$D_2$ is ON ad $D_1$ is OFF**

**Then the circuit can be replaced by**




**Find the current through $D_2$**

$$I = \frac{10 - 0.3}{1000 + 20} = 9.51\ mA$$

**So the voltage $V_{AB}$ can be written as**

$$V_{AB} = 20 \times 9.51mA + 0.3$$

$$V_{AB} = 0.49\ V$$

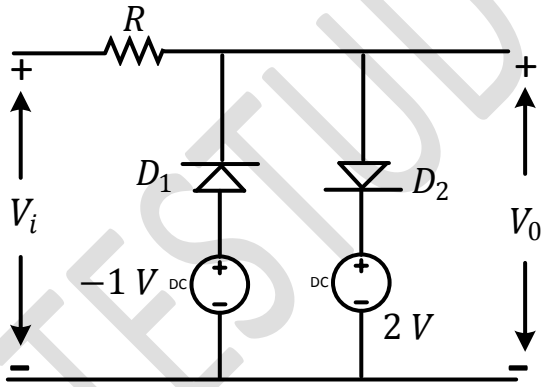
**Since $V_{AB}$ or $V_{D1}$ is 0.49 V**

**Which is less than 0.7 V**

**So $D_1$ is non conducting**

**Option (d)**

19. Two silicon diodes, with a forward voltage drop of 0.7 V, are used in the circuit shown in the figure. The range of input voltage $V_i$ for which the output voltage $V_0 = V_i$ , is




(a) $-0.3\ V < V_i < 1.3\ V$
(b) $-0.3\ V < V_i < 2\ V$
(c) $-1.0\ V < V_i < 2.0\ V$
(d) $-1.7\ V < V_i < 2.7\ V$

**[GATE 2014: 1 Mark]**

**Soln. When $V_i \geq 2.7\ V$ then**

**$D_2$ is for forward biased and**

**$D_1$ is Reverse Biased**

**So,**

$$V_0 = V_i$$

**When**

$V_i < 2.7\ V$ , $D_i$ **is Reverse biased** $and\ D_2$ **is also Reverse biased**

$So, V_0 = V_i$

$If\ V_i \leq -1.7\ V\ then\ D_1\ get\ F.B$

$If\ V_i \geq -1.7\ V\ then\ D_1\ is\ no\ F.B\ and\ D_2\ is\ R.B$

$So, V_0 = V_i$

**Thus for the Option (d) i.e.**

$-1.7\ V < V_i < 2.7\ V$

$V_0 = V_i$

**Option (d)**

20. A region of negative differential resistance is observed in the current voltage characteristics of a silicon PN junction if
(a) both the P – region and the N – region are heavily doped
(b) the N – region is heavily doped compared to the P – region
(c) the P – region is heavily doped compared to the N – region
(d) an intrinsic silicon region is inserted between the P – region an d N – region

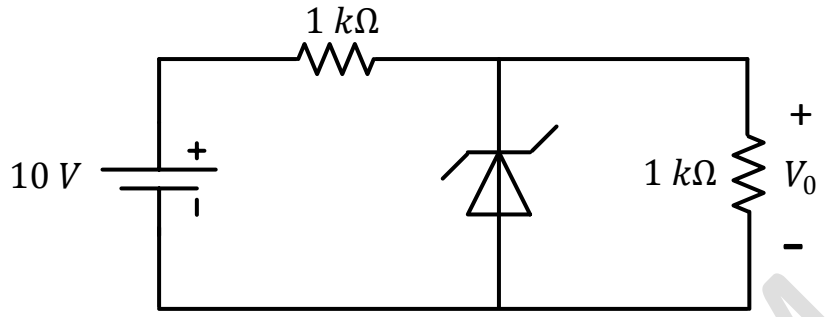
**[GATE 2015: 1 Mark]**

**Soln. The negative resistance is observed in the current voltage characteristics of the P N Junction in the case of Tunnel Diodes.**

**P and N region in Tunnel Diodes are degenerate i.e. heavily doped with impurities. When no voltage is applied to the diode, due to high doping, depletion region is very narrow thus tunnelling distance is very narrow (5 – 10 nm). When forward bias is a applied, there exists a band of energy states that are occupied on the n side and corresponding band of energy states is available and unoccupied on p side. The electrons tunnel from n side to p side and give rise to negative resistance.**

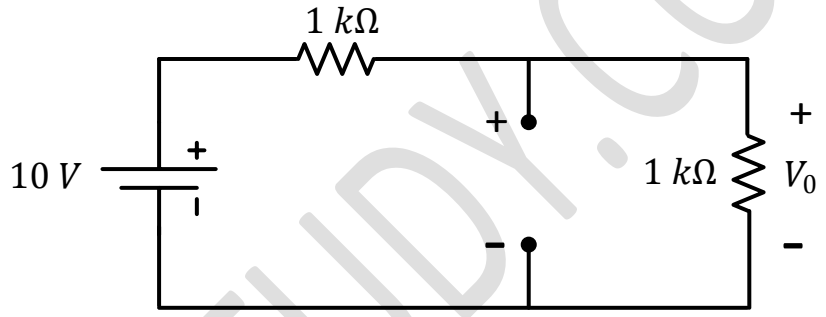
**Option (a)**

21. In the circuit shown below, the Zener diode is ideal and the Zener voltage is 6V. The output voltage $V_0$ (in volts) is _____.




**[GATE 2015: 1 Mark]**

**Soln.** **In the given circuit we can find the voltage across Zener diode which is reverse biased**




**Voltage across Zener diode (V)**

$$\boldsymbol{V = \frac{10 \times 1K}{1K + 1K} = 5V}$$

**Thus the voltage across the Zener diode is less than the breakdown voltage (given as 6V)**

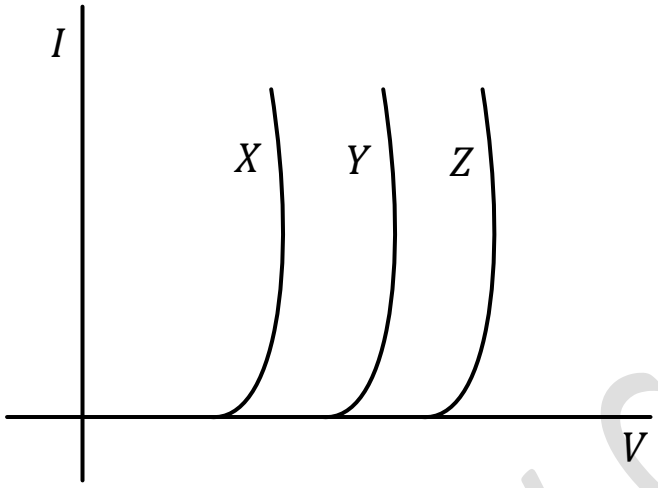
**i.e.** $\mathbf{V < V_z}$

**So, Zener diode will be reverse biased**

**So,** $\boldsymbol{V_0 = V = 5V}$

**Answer 5 V**

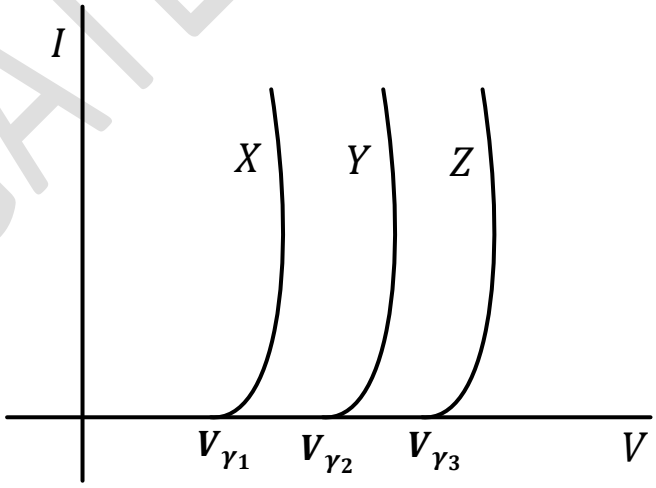
22. The I – V characteristics of three types of diodes at the room temperature, made of semiconductor X, Y and Z, are shown in the figure. Assume that the diodes are uniformly doped and identical in all respects except their materials. If $E_{gX}$, $E_{gY}$ and $E_{gZ}$ the band gaps of X, Y and Z, respectively, then




(a) $E_{gX} > E_{gY} > E_{gZ}$
(b) $E_{gX} = E_{gY} = E_{gZ}$
(c) $E_{gX} < E_{gY} < E_{gZ}$
(d) no relationship among these band gaps exists.

**[GATE 2016: 1 Mark]**

**Soln. In the given figure forward characteristics of three types of diodes is given. Here $V_\gamma$ is the cut in voltage.**




**In the given figure**

$$V_{\gamma_3} > V_{\gamma_2} > V_{\gamma_1}$$

**If band gap is large the intrinsic concentration of electron ($n_i$) will be small**

**Cut- in voltage is given by**

$$V_\gamma = K\,T\,ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$So, \quad V_\gamma \propto E_g$$

$$So, \quad E_{gZ} > E_{gY} > E_{gX}$$

**Option (c)**