

MOSFET & IC Basics - GATE Problems (Part - I)

1. Channel current is reduced on application of a more positive voltage to the GATE of the depletion mode n – channel MOSFET. (True/False)

[GATE 1994: 1 Mark]

Soln. The MOSFET is of depletion mode and n – channel type. Like JFET, depletion mode MOSFET is normally ON device. i.e. has drain current when $V_{GS} = 0\text{ V}$

In depletion mode MOSFETs drain current can exceed I_{DSS} (not like JFETs) if the gate voltage is of correct polarity to increase number of charge carriers in the channel.

For n – channel D – MOSFET, I_D is greater than I_{DSS} when V_{GS} is positive. Since with more +ve voltage the channel becomes more n – type

Thus, false

2. MOSFET can be used as a
 - (a) Current controlled capacitor
 - (b) Voltage controlled capacitor
 - (c) Current controlled inductor
 - (d) Voltage controlled inductor

[GATE 2001: 1 Mark]

Soln. The MOS capacitor is the heart of MOSFET.

The capacitance of the device is defined as

$$C = \frac{dQ}{dV}$$

Where dQ is differential change in charge on one plate as a function of dV .

Thus, it can be used as voltage controlled capacitor

Option (b)

3. The effective channel length of a MOSFET in saturation decreases with increase in
- (a) Gate voltage
 - (b) Drain voltage
 - (c) Source voltage
 - (d) Body voltage

[GATE 2001: 1 Mark]

Soln. In a MOSFET at the onset of saturation i.e. when drain to source voltage reaches V_{DSat} the inversion layer charge at the drain end becomes zero (ideally). The channel is said to be pinched off at the drain end.

If drain to source voltage V_{DS} is increased even further beyond the saturation i.e. $V_{DS} > V_{DSat}$ an even larger portion of the channel becomes pinched off, and effective channel length is reduced.

(REF: Streetman)

Option (b)

4. For an n – channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk (i.e. $V_{SB} > 0$), the threshold voltage V_T of the MOSFET will
- (a) Remain unchanged
 - (b) Decrease
 - (c) Change polarity
 - (d) Increase

[GATE 2003: 1 Mark]

Soln. So for we considered that substrate or body is connected to source and held at ground.

$$V_{SB} \geq 0$$

For n – channel device V_{SB} be +ve i.e. (change in threshold voltage) ΔV_T is always positive. So as $V_{SB} > 0$, the V_T will increase.

REF: NEAMAN

Option (d)

5. A MOS Capacitor made using p – type substrate is in accumulation mode. The dominant charge in the channel is due to the presence of
- (a) Holes
 - (b) Electrons
 - (c) Positively charged ions
 - (d) Negatively charged ions

Soln. MOS Capacitor is made using p – type substrate when gate is supplied with negative voltage i.e. $V_{GS} < 0$. It will be in accumulation mode. In this case it attracts holes beneath the gate, therefore the charge in the channel is due to holes.

Option (a)

6. The drain current of a MOSFET in saturation is given by

$I_D = K (V_{GS} - V_T)^2$, where K is a constant. The magnitude of the transconductance g_m is

(a) $\frac{K(V_{GS}-V_T)^2}{V_{DS}}$

(b) $2K(V_{GS} - V_T)$

(c) $\frac{I_D}{V_{GS}-V_{DS}}$

(d) $\frac{K(V_{GS}-V_T)^2}{V_{GS}}$

[GATE 2008: 1 Mark]

Soln. Given,

Drain current of MOSFET in saturation

$$I_D = K (V_{GS} - V_T)^2$$

Since,

$$\text{Transconductance } (g_m) = \frac{\partial I_D}{\partial V_{GS}}$$

$$\frac{\partial I_D}{\partial V_{GS}} = K \cdot 2 \cdot (V_{gs} - V_T)$$

$$= 2K(V_{gs} - V_T)$$

Option (b)

7. At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon n – channel MOSFET is

(a) $450 \text{ cm}^2 / \text{V} - \text{s}$

(b) $1350 \text{ cm}^2 / \text{V} - \text{s}$

(c) $1800 \text{ cm}^2 / \text{V} - \text{s}$

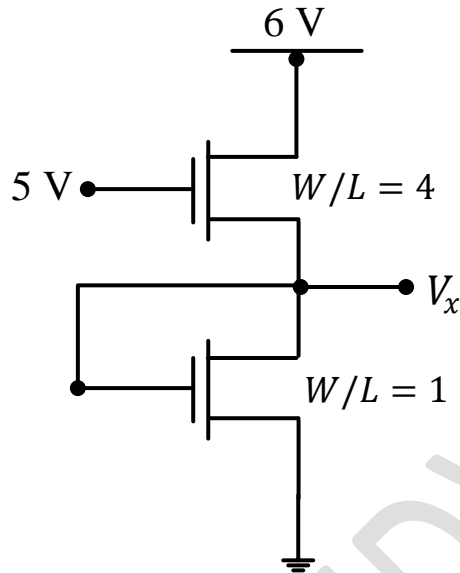
(d) $3600 \text{ cm}^2 / \text{V} - \text{s}$

[GATE 2010: 1 Mark]

Soln. The mobility of electrons is the standard value, it will be same for electrons in the inversion layer

Option (b)

8. In the circuit shown below. For the MOS transistors, $\mu_n C_{OX} = 100 \mu A/V^2$ and the threshold voltage $V_T = 1$ V. The voltage V_X at the source of the upper transistor is



- (a) 1 V
(b) 2 V

- (c) 3 V
(d) 3.6 V

[GATE 2011: 1 Mark]

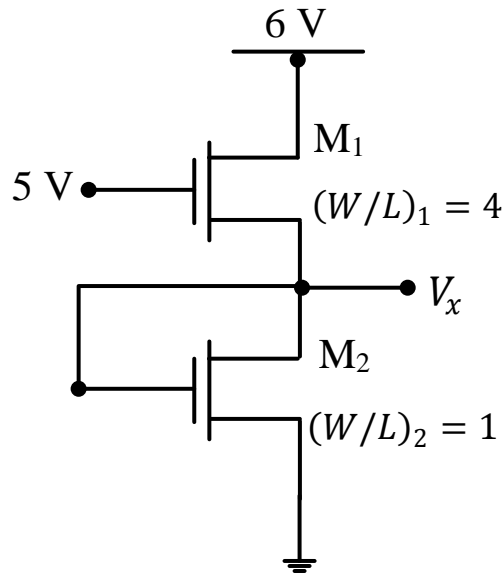
Soln. Assume, Top MOSFET as M_1

Bottom MOSFET as M_2

M_1 is in saturation since

$$V_G > V_T \text{ (Here } V_G \text{ is 5 V and } V_T \text{ is 1 V)}$$

Since MOSFET are connected in series the same current will flow through M_2



Drain current for M_1 in saturation is

$$I_{DS1} = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2$$

Similarly for M_2

$$I_{DS2} = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2$$

Since,

$$I_{DS1} = I_{DS2}$$

$$\left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2 = \left(\frac{W}{L}\right)_2 (V_{GS2} - V_T)^2$$

$$V_{GS1} = V_G - V_x = 5 - V_x$$

$$4(5 - V_x - V_T)^2 = 1 \cdot (V_x - V_T)^2$$

$$\text{or, } 2(5 - V_x - V_T) = (V_x - V_T)$$

$$\text{or, } V_x = 3V$$

$$\text{Answer:- } V_x = 3V$$

9. In a MOSFET operating in the saturation region, the channel length modulation effect causes
- (a) An increase in the gate – source capacitance
 - (b) A decrease in the transconductance
 - (c) A decrease in the unity – gain cut – off frequency
 - (d) A decrease in the output resistance

[GATE 2013: 1 Mark]

Soln. For a MOSFET operating in saturation region the channel length modulation effect causes a decrease in output resistance. The drain characteristics becomes less flat.

Option (d)

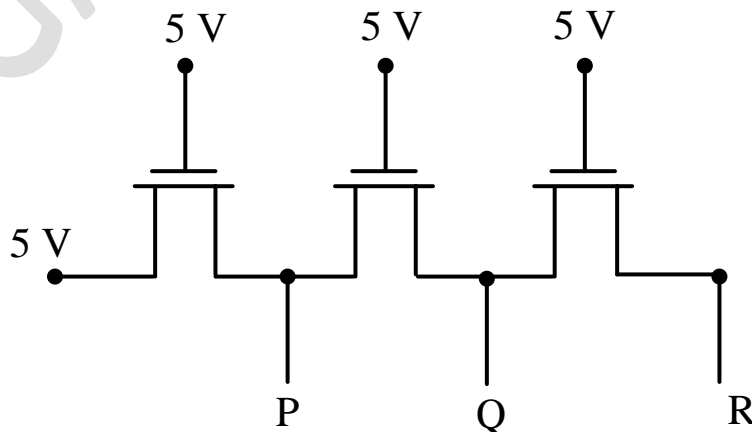
10. In IC technology, dry oxidation (using dry oxygen) as compared to wet oxidation (using steam or water vapour) produces
- (a) Superior quality oxide with a higher growth rate
 - (b) Inferior quality oxide with a higher growth rate
 - (c) Inferior quality oxide with a lower growth rate
 - (d) Superior quality oxide with a lower growth rate

[GATE 2013: 1 Mark]

Soln. A superior quality oxide layer is formed with dry oxidation but with a lower growth rate.

Option (d)

11. In following circuit employing pass transistor logic, all NMOS transistor are identical with a threshold voltage of 1V. Ignoring the body – effect, the output out-put voltage at P, Q and R are

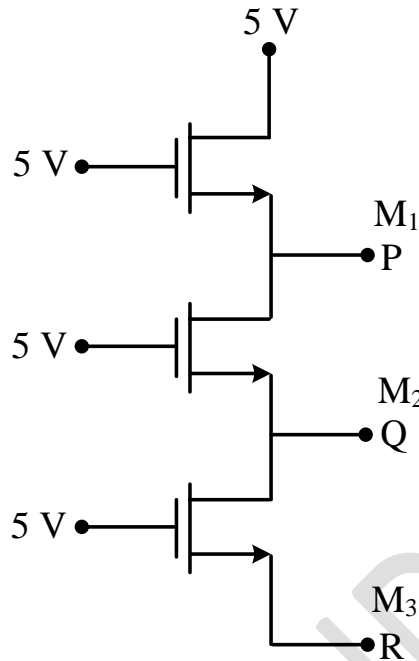


- (a) 4 V, 3 V, 2 V
 (b) 5 V, 5 V, 5 V

- (c) 4 V, 4 V, 4 V
 (d) 5 V, 4 V, 3 V

[GATE 2014: 1 Mark]

Soln. Assume all NMOS are in saturation



$$V_{DS} \geq (V_{GS} - V_T)$$

For M₁:

$$(5 - V_P) \geq (5 - V_P - 1)$$

$$\text{or, } 5 - V_P > 4 - V_P$$

Thus in saturation

$$I_{D1} = k(V_{GS} - V_T)^2$$

$$\text{or, } I_{D1} = K(4 - V_P)^2 \text{ --- (1)}$$

For M₂:

$$I_{D2} = K(5 - V_Q - 1)^2$$

$$\text{or, } I_{D2} = K(4 - V_Q)^2 \text{ --- (2)}$$

Since $I_{D1} = I_{D2}$

$$(4 - V_P)^2 = (4 - V_Q)^2$$

$$\text{or, } V_P = V_Q \quad \text{and} \quad V_P + V_Q = 8$$

$$\text{or, } V_P = V_Q = 4V$$

For M₃:

$$I_{D3} = K(5 - V_R - 1)^2$$

$$\text{or, } I_{D2} = I_{D3}$$

$$(4 - V_Q)^2 = (4 - V_R)^2$$

$$\text{or, } V_R = V_Q = 4V$$

$$\text{Thus, } V_P = V_Q = V_R = 4V$$

Option (c)

12. If fixed positive charges are present in the gate oxide of an n – channel enhancement type MOSFET, it will lead to
- (a) A decrease in the threshold voltage
 - (b) Channel length modulation
 - (c) An increase in substrate leakage current
 - (d) An increase in accumulation capacitance

[GATE 2014: 1 Mark]

Soln. In n – channel enhancement type MOSFET, a positive voltage is applied at the gate which creates channel between source and drain.

In the problem it is given that fixed positive charges are present in the gate oxide, it will make easier to create the channel between source and drain. Hence the threshold voltage will decrease.

Option (a)

13. In CMOS technology, shallow P – well or N – well regions can be formed using
- (a) Low pressure chemical vapour deposition
 - (b) Low energy sputtering
 - (c) Low temperature dry oxidation
 - (d) Low energy ion – implantation

[GATE 2014: 1 Mark]

Soln. In triple well CMOS process a deep n – well is first driven into the p – type substrate, and is used as shielding frame against disturbances from the substrate and provides N – channel MOSFET with better insulation from noise. The process used is low energy ion implantation.

Option (d)

14. In MOSFET fabrication, the channel length is defined during the process of
- (a) Isolation oxide growth
 - (b) Channel stop implantation
 - (c) Poly – silicon gate patterning
 - (d) Lithography step leading to the contact pads

[GATE 2014: 1 Mark]

Soln. In MOSFET fabrication channel length is defined during Poly – silicon gate patterning process.

Option (c)

15. Which one of the following processes is preferred to form the gate dielectric (SiO_2) of MOSFETs?
- (a) Sputtering
 - (b) Molecular beam epitaxy
 - (c) Wet oxidation
 - (d) Dry oxidation

[GATE 2015: 1 Mark]

Soln. In wet oxidation where water is used instead of oxidation process has significantly greater oxidation rate than dry oxidation. It is used to grow thick oxides such as masking oxides.

Dry oxidation has a lower growth rate than wet oxidation although oxide film quality is better than wet oxide film. It is used in transistor gates and capacitances and especially in gate oxide in MOSFETs

Option (d)

16. Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET):
- P: As channel length reduces, OFF – state current increases.
 - Q: As channel length reduces, output resistance increases.
 - R: As channel length reduces, threshold voltage remains constant.

- S: As channel reduces, ON current increases.
Which of the above statements are INCORRECT?
- (a) P and Q
 - (b) P and S
 - (c) Q and R
 - (d) R and S

[GATE 2016: 1 Mark]

Soln. P: As channel length reduces, OFF state current increases.

The drain current is in saturation since it does not increase, but when channel length is reduced the drain current will increase slightly.

This effect is called drain induced barrier lowering (DIBL). This state is the OFF state (High resistance state): So, it is TRUE

Q: As channel length reduces output resistance increases.

The output resistance reduces with channel length reduction

So, TRUE

R: As channel length reduces, threshold voltage remains constant.

As channel length reduces.

S: As channel reduces, ON current increases

TRUE

Option (c)

17. A long – channel NMOS transistor is biased in the liner region $V_{DS} = 50\text{ mV}$ and is used as a resistance. Which one of the following statements is NOT correct?

- (a) If the device width W is increased, the resistance decrease.
- (b) If the threshold voltage is reduced, the resistance decreases.
- (c) If the device length L is increased, the resistance.
- (d) If V_{GS} is increased, the resistance increases.

[GATE 2016: 1 Mark]

Soln. Liner region of NMOS is the region of low resistance (on region). The equation is

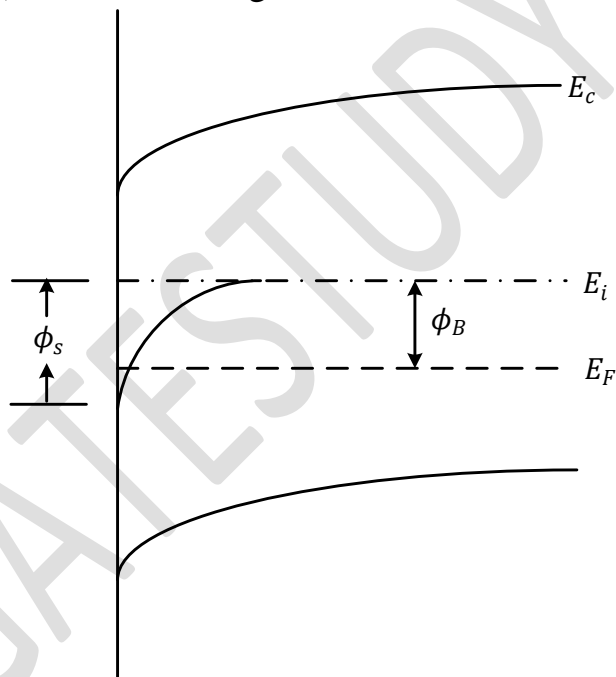
$$r_{ds(on)} = \frac{1}{\mu_n C_{OX} \cdot \frac{W}{L} [V_{GS} - V_T]}$$

Thus, as per above equation

- A: TRUE
- B: TRUE
- C: TRUE
- D: FALSE

Option (d) is correct

18. The figure shows the band diagram of a Metal Oxide Semiconductor (MOS). The surface region of this MOS is in



- (a) Inversion
- (b) Accumulation
- (c) Depletion
- (d) Flat band

[GATE 2016: 1 Mark]

Soln. The given band diagram of a Metal Oxide Semiconductor.

Note that Fermi level of semiconductor is between intrinsic level and conduction level (near to E_c) so the semiconductor is of n – type.

Whenever surface potential (ϕ_s) is larger than, QB surface is inverted.

Thus the surface region of MOS is in inversion.

Option (a)

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