MOSFET & IC Basics – GATE Problems (Part - II)

1. In MOSFET devices the N-channel type is better than the P – Channel type in the following respects.
   (a) It has better immunity
   (b) It is faster
   (c) It is TTL compatible
   (d) It has better drive capability

[GATE 1988: 2 Marks]

Soln. **In N – Channel MOSFETs the charge carriers are electrons while in P – channel MOSFETs holes are the charge carriers.**

The mobility of electrons is always greater than the mobility of holes.

i.e. $\mu_n > \mu_p$

Thus, N – Channel MOSFETs are faster

Option (b)

2. In a MOSFET, the polarity of the inversion layer is the same as that of the
   (a) Charge on the GATE – EC – electrode
   (b) Minority carries in the drain
   (c) Majority carriers in the substrate
   (d) Majority carries in the source

[GATE 1989: 2 Marks]

Soln. **In a MOSFET the polarity of inversion layer is the same as that of majority carriers in the source.**

For example, for N – MOSFETs the source is of N – type and inversion layer formed is of electrons.

Option (d)

3. Which of the following effects can be caused by a rise in the temperature?
   (a) Increase in MOSFET current (I_{DS})
   (b) Increase in BJT current (I_C)
   (c) Decrease in MOSFET current (I_{DS})
   (d) Decrease in BJT current (I_C)

[GATE 1990: 2 Marks]

Soln. The current equation for BJT is

$$I_C = \beta\, I_b + (1+\beta) I_{CO}$$

As temperature increases, the leakage current I_{CO} increases, so the current I_C increases in BJT.

Since mobility decreases as temperature increases. So in MOSFETs current I_{DS} decreases with rise in temperature

Option (b) and (c)

4. When the gate – to – source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400 mV is

(a) 0.5 mA (c) 3.5 mA

(b) 2.0 mA (d) 4.0 mA

[GATE 2003: 2 Marks]

Soln. Given,

$$V_T = 400\ mV = 0.4\ V$$

Voltage applied at gate

$V_{GS} = 900\ mV$ **=0.9 V**

$$I_{DS} = 1\ mA$$

Find the drain current for

$$V_{GS} = 1400\ mV$$

MOSFET is operating in saturation

$$I_{DS} = K\,(V_{GS} - V_T)^2$$

$$or,\ 1 \times 10^{-3} = K\,(0.9 - 0.4)^2$$

$$or,\quad K = \frac{10^{-3}}{(0.5)^2} = 4 \times 10^{-3}\ \frac{A}{V^2}$$

For V_{GS} = 1.4 V

$$I_{DS} = K\,(V_{GS} - V_T)^2$$

$$= 4 \times 10^{-3}\,(1.4 - 0.4)^2$$

$$I_{DS} = 4\ mA$$

Option (d)

5. The drain of an n – channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of MOSFET is 1 V. If the drain current (I_D) is 1 mA for V_{GS} = 2 V, then for $V_{GS} = 3\ V$, I_D is
   (a) 2 mA (c) 9 mA
   (b) 3 mA (d) 4 mA

[GATE 2004: 2 Marks]

Soln. Given,

$$V_{GS} = V_{DS}$$

Then the device is in saturation.

So, $I_{DS} = K\ (V_{GS} - V_T)^2$

For $I_{DS} = 1\ mA$, $V_{GS} = 2V$, $V_T = 1V$

$$1 = K\ (2 - 1)^2$$

$$or,\ K = 1\ mA/V^2$$

Again,

$$I_D = K\ (V_{GS} - V_T)^2$$

For $V_{GS} = 3\ V$

$$I_D = 1 \times (3 - 1)^2$$

$$I_D = 4\ mA$$

Option (d)

6. An n – channel depletion MOSFET has following two points on its $I_D - V_{GS}$ curve
   (i) $V_{GS} = 0 \quad at \quad I_D = 12\ mA \quad and$
   (ii) $V_{GS} = -6\ V \quad at \quad I_D = 0$

   Which of the following Q point will give the highest transconductance gain for small signals?

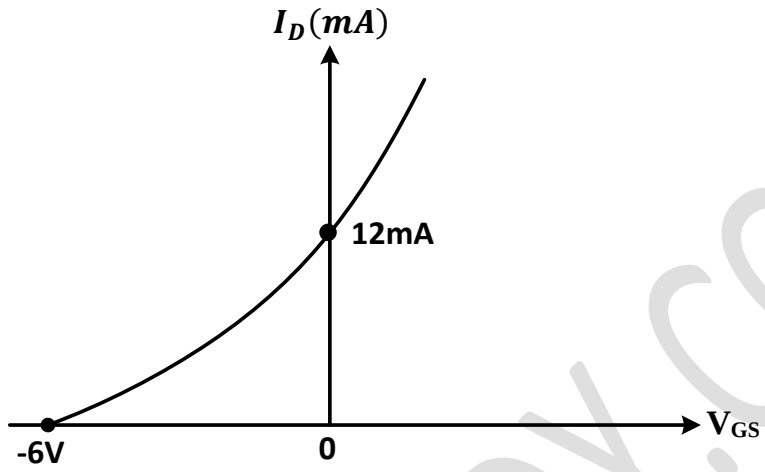
(a) $V_{GS} = -6\ V$ (c) $V_{GS} = 0\ V$

(b) $V_{GS} = -3\ V$ (d) $V_{GS} = 3\ V$

[GATE 2006: 2 Marks]

Soln. **Transconductance** $(g_m) = \frac{\delta I_D}{\delta V_{GS}}$ **for** $V_{DS} = constant$

The characteristics is plotted.



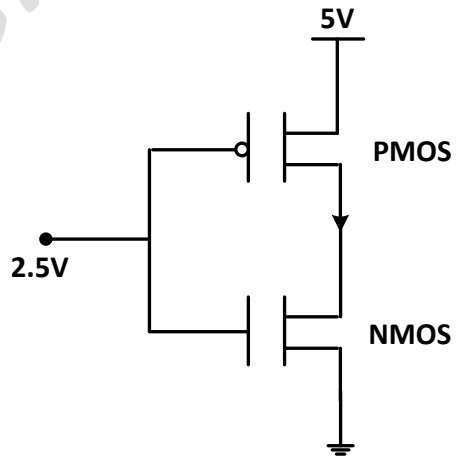
As I_D increases V_{GS} also increases Larger V_{GS} will have high transconductance

Thus, Option (d)

7. In the C MOS inverter circuit shown if the transconductance parameters of N MOS and P MOS transistor are

$$K_n = K_p = \mu_n C_{OX} \frac{W_n}{L_n} = \mu_p C_{OX} \frac{W_p}{L_p} = 40\ \mu A/V^2$$

and threshold voltages are $V_T = 1V$ the current I is



(a) 0 A
(b) 25 µA
(c) 45 µA
(d) 90 µA

[GATE 2007: 2 Marks]

Soln. Given

$$K_n = K_p = 40\ \mu A/V^2$$

$$V_T = 1\ V$$

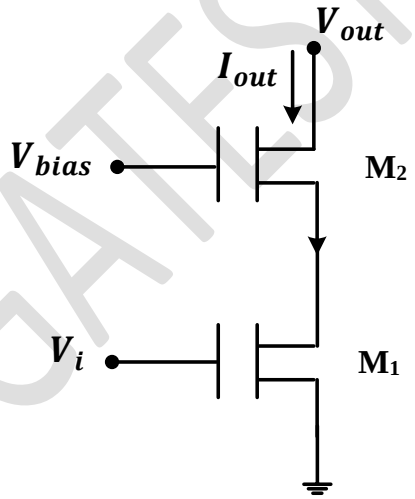
The device is in saturation. So the current is given by

$$I_{DS} = \frac{K_n}{2}\ (V_{GS} - V_T)^2$$

$$\frac{40}{2}(2.5 - 1)^2 = 20 \times (1.5)^2 = 45\ \mu A$$

Option (c)

8. Two identical N MOS transistors M_1 and M_2 are connected as shown below. V_{bias} Chosen so that both transistor are in saturation. The equivalents g_m of the pair is defined to be $\frac{\partial\, I_{out}}{\partial\, V_i}$ at constantV_{out}. The equivalent g_m of the pair is



(a) The sum of individual g_m of two transistors.
(b) The product of individual g_m of the transistors.
(c) Nearly equal to the g_m of M_1
(d) Nearly equal to g_m/g_0 of M_2

[GATE 2008: 2 Marks]

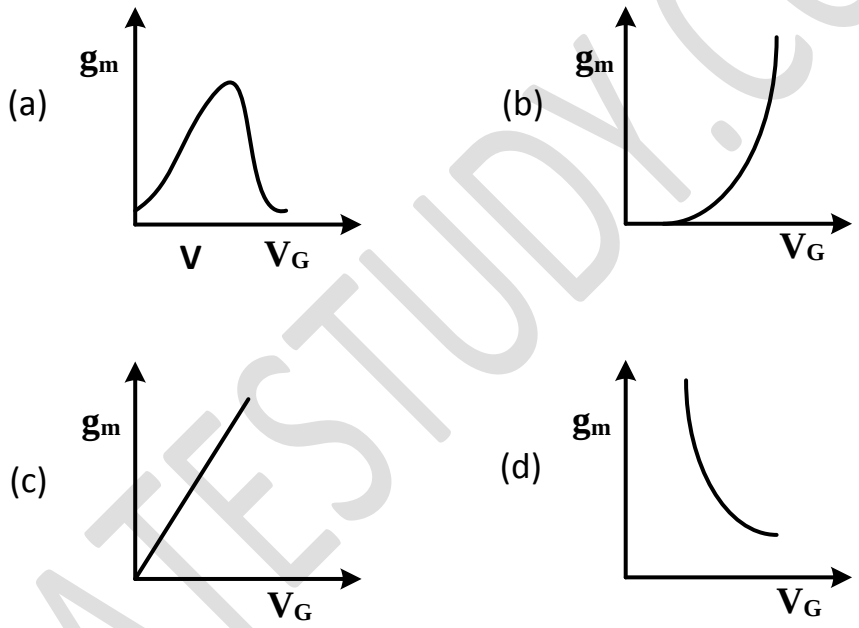
Soln. As per the principle of transconductance

$$\frac{1}{g_m} = \frac{1}{g_{m_1}} = \frac{1}{g_{m_2}}$$

$$or, \quad g_m = \frac{g_{m_1} g_{m_2}}{g_{m_1} + g_{m_2}} \cong g_{m_1}$$

Option (c)

9. The measured Transconductance g_m of an NMOS transistor operating in the linear region is plotted against voltage V_G at a Constant drain voltage V_D. Which of the following figures represents the expected dependence of g_m on V_G .



[GATE 2008: 2 Marks]

Soln. Drain current I_D in the linear region is given by

$$I_D = K_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$and \quad g_m = \frac{\partial I_D}{\partial V_{GS}} = K_n (V_{GS} - V_T) V_{DS}$$

$$So, \quad g_m \propto V_{GS}$$

So, linear characteristic

Option (c)

10. Consider the following two situations about the internal conditions in an n – channel MOSFET operating in the active region.

S_1: The inversion charge decreases from source to drain

S_2 : The channel potential increases from source to drain

Which of the following is correct?

(a) Only S_2 is true

(b) Both S_1 and S_2 are false

(c) Both S_1 and S_2 are true but S_2 is not a reason for S_1

(d) Both S_1 and S_2 are true and S_2 is reason for S_1

[GATE 2009: 2 Marks]

Soln. MOSFET is also considered as gate – controlled resistor.

When +ve gate voltage in an n – channel MOSFET exceeds V_T, electrons are induced in p – type substrate. This channel is also connected to n^+ source and drain regions. Channel looks like induced n – type resistor. With increase in gate voltage the channel becomes more conducting. The drain current increase (linear region). When more drain current flows, there is more ohmic voltage drop along the channel. The channel potential varies near zero from source to the potential at drain end.

The voltage difference between gate and channel reduces from V_G (near source) to $(V_G - V_D)$ near drain. When drain bias is increased $(V_G - V_D) = V_T$, the channel is piched off. When V_D increase further the drain current is in saturation.

So, S_1 & S_2 are true and S_2 is reason for S_1

Option (d) **(Refer: Streetman)**

11. The source of a silicon ($n_i = 10^{10}\ per\ cm^3$) n – channel MOS transistor has an area 1 sq μm and a depth of 1 μm. If the dopant density in the source is $10^{19}/cm^3$ the no. of holes in the source region with above volume is approx.

(a) 10^7 (c) 10

(b) 100 (d) 0

[GATE 2012: 2 Marks]

Soln. Given,

$$n_i = 10^{10}/cm^3$$

$$Area \quad (A) = 1 \times 10^{-12}/m^2$$

$$depth \quad (d) = 10^{-6}\ m$$

$$Volume = A \,.\, d = 1 \times 10^{-2} \times 10^{6}\ \ m^3$$

$$= 10^{-18}/m^3$$

$$= 10^{-12}/cm^3$$

$$N_D = n = 10^{19}/cm^3$$

$$p = \frac{n_i^2}{N_D} = \frac{10^{20}}{10^{19}} = 10/cm^3$$

So,

Holes in volume V is

$$H = p \,.\, V = 10^{-12} \times 10$$

$$= 10^{-11}$$

Since not integer number $\cong 0$

Option (d)

12. A depletion type N – channel MOSFET in biased in its linear region for use as a voltage controlled resistor . Assume threshold voltage $V_{TH} = 0.5V$, $V_{GS} = 2.0V$, $V_{DS} = 5V$, $W/L = 100$, $C_{OX} = 10^{-8}\ F/cm^2$ and $\mu_n = 800\ cm^2/V - s$. The value of the resistance of the voltage controlled resistor $(in\ \Omega)$ is _____

[GATE 2014: 2 Marks]

Soln. Given,

Depletion type MOSFET (N – Channel)

In linear region

$$V_{TH} = 0.5V$$

$$V_{GS} = 2.0V$$

$$V_{DS} = 5V$$

$$W/L = 100$$

$$C_{OX} = 10^{-8}\ F/cm^2$$

The value of voltage controlled resistor is given by

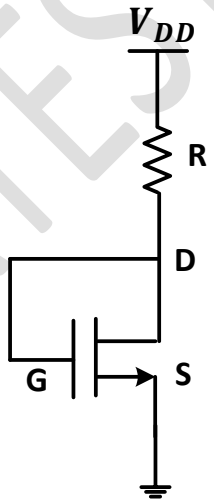
$$r_{ds} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_T)}$$

$$r_{DS} = \frac{1}{800 \times 10^{-8} \times 100[2 - (-0.5)]}$$

$$r_{DS} = 500\ \Omega$$

Answer: 500 Ω

13. For the n – channel MOS transistor shown in figure, the threshold voltage V_{TH} is 0.8V. Neglect channel length modulation effects. When the drain voltage V_D = 1.6, the drain current I_D was found to be 0.5 mA. If V_D is adjusted to be 2V by changing the values of R and V_{DD}, the new value of I_D (in m A) is



(a) 0.625
(b) 0.75
(c) 1.125
(d) 1.5

[GATE 2014: 2 Marks]

Soln. Given,

$$V_{TH} = 0.8\,V$$

$$V_D = 1.6\,V$$

$$I_D = 0.5\,mA$$

For the given figure we notice that Gate is connected to drain

So, $V_{GS} = V_{DS} = V_D$

In saturation I_D is given by

$$I_{DS} = K(V_{GS} - V_T)^2$$

$$So, \qquad \frac{I_{D_2}}{I_{D_1}} = \frac{\left[V_{GS_2} - V_T\right]^2}{\left[V_{GS_1} - V_T\right]^2}$$

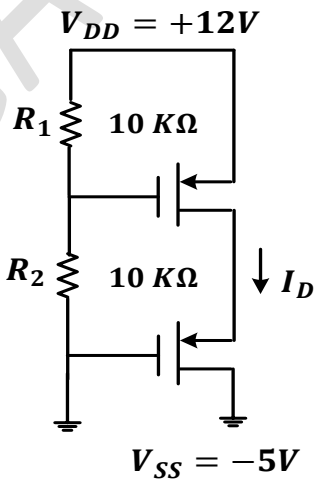
$$So, \qquad \frac{I_{D_2}}{I_{D_1}} = \frac{(2-0.8)^2}{(1.6-0.8)^2} = 2.25$$

$$or, \qquad I_{D_2} = 2.25 \times 0.5$$

$$= 1.125\,mA$$

Option (c)

14. For the MOSFET shown in the figure the threshold voltage $|V_t| = 2V$ and $K = \frac{1}{2}\mu c\left(\frac{W}{L}\right) = 0.1mA/V^2$. The value of I_D (in mA) is _____



[GATE 2014: 2 Marks]

Soln. The two MOSFET are in series so, same current will be flowing. For the bottom MOSFET it is easier to find V_{GS}

$$V_{GS} = V_G - V_S = 0 — 5$$

$$= 5V$$

V_{GS} is greater than threshold voltage,

So, MOSFET is in saturation

$$I_D = \frac{1}{2}\,\mu_n\, C_{OX}\frac{W}{L}[V_{GS} - V_T]^2$$

$$= 0.1\ mA/V^2\ [5-2]^2$$

$$0.1\ mA/V^2\ [3]^2$$

$$I_D = 0.9\ mA$$

Answer: 0.9 mA

15. The slope of the $I_D\ vs\ .V_{GS}$ curve of an n – channel MOSFET in linear region is $10^{-3}\ \Omega^{-1}$ at $V_{DS} = 0.1V$. For the same device, neglecting channel length modulation, the slope of the $\sqrt{I_D}\ vs\ V_{GS}$ curve $(in\ \sqrt{A}/V)$ under saturation region is approximately _____

[GATE 2014: 2 Marks]

Soln. Given,

Slope of $I_D\ vs\ .V_{GS}$ curve for N – MOSFET in linear region is $10^{-3}\ \Omega^{-1}$

$$i.e.\quad \frac{\partial\, I_D}{\partial\, V_{GS}} = 10^{-3}$$

In linear region the drain current is given by

$$I_D = K_n\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}\,V_{DS}^2\right]$$

$$where\ \ K_n = \mu_n\, C_{OX}\frac{W}{L}$$

$$\frac{\partial I_D}{\partial V_{GS}} = K_n V_{DS}$$

$$or,\ \ K_n = \frac{\frac{\partial I_D}{\partial V_{GS}}}{V_{DS}} = \frac{10^{-3}}{0.1} = 10^{-2}$$

For saturation region

$$I_D = \frac{1}{2} K_n [V_{GS} - V_T]^2$$

$$or,\ \ \sqrt{I_D} = \sqrt{\frac{K_n}{2}} [V_{GS} - V_T]$$

$$\frac{\partial \sqrt{I_D}}{\partial V_{GS}} = \sqrt{\frac{K_n}{2}}$$

$$or,\ \ \frac{\partial \sqrt{I_D}}{\partial V_{GS}} = \sqrt{\frac{10^{-2}}{2}} = 0.0707 \sqrt{A} / V$$

Answer: $0.0707 \sqrt{A} / V$

16. An ideal MOS capacitor has boron doping concentration of $10^{15}\ cm^{-3}$ in the substrate. When a gate voltage is applied, a depletion region of width 0.5 μm is formed with a surface (channel) potential of 0.2 V. Given that $\in_0 = 8.854 \times 10^{-14}$F/cm and the relative permittivity of silicon and silicon dioxide are 12 and 4 respectively the peak electric filed in $V/\mu m$ in the oxide region is _____

[GATE 2014: 2 Marks]

Soln. Dopant is Boron, so p – type substrate

Thus device is n MOSFET. Peak electric field in S_i substrate

$$E_{si} = \frac{2\Psi_s}{W_d}$$

Where, $\Psi_s - surface\ potential$

$W_d - depletion\ region\ width$

$$E_{si} = \frac{2 \times 0.2}{0.5\mu m} = 0.8/\mu m$$

Electric field in oxide

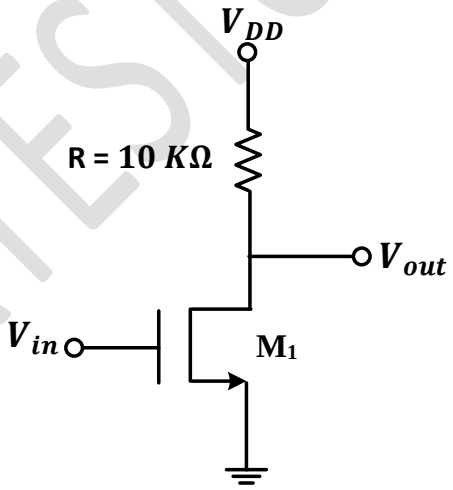
$$E_{OX} = \frac{\in_s}{\in_{OX}} . E_{si}$$

$$= \frac{12}{4} \times 0.8V/\mu m$$

$$= 2.4\,V/\mu m$$

Answer: $E_{OX} = 2.4V/\mu m$

17. For the MOSFET M_1 shown in figure, assume $W/L = 2, V_{DD} = 2.0V, \mu_n\, C_{OX} = 100\ \mu m/V^2\ and\ V_{TH} = 0.5V$. The transistor M_1 switches from saturation region to linear region when V_{in} (in volts) is _____



[GATE 2014: 2 Marks]

Soln. For saturation region drain current is given by

$$I_D = K_n[V_{GS} - V_T]^2$$

$$= \frac{1}{2}\mu_n C_{OX} \frac{W}{L}[V_{GS} - V_T]^2$$

$$= \frac{1}{2}\mu_n C_{OX}\frac{W}{L}[V_0]^2$$

$$since, \quad V_{GS} - V_T = V_{DS} = V_0$$

$$So, \quad I_D = \frac{1}{2} \times 100 \times 10^{-6} \times 2 \times V_0^2$$

$$or, \quad I_D = 100 \times 10^{-6}\, V_0^2 \; ---------- (1)$$

Applying KVL in outer loop

$$V_{DD} = I_D \times 10K + V_0 \; ---------- (2)$$

From equation (1) and (2) we get

$$2 = 100 \times 10^{-6}\, V_0^2 + V_0$$

$$or, \quad 2 = V_0^2 + V_0$$

$$or, \quad V_0^2 + V_0 - 2 = 0$$

$$V_0 = \frac{-1 \pm \sqrt{1 + 4 \times 1 \times 2}}{2 \times 1} = \frac{-1 \pm 3}{2}$$

$$So, \quad V_0 = 1V \; or \; -2V$$

Taking $V_0 = 1V$

$$V_{DS} = V_{GS} = V_T$$

$$or, \quad V_0 = V_{in} - V_T$$

$$or, \quad V_{in} = 1 + 0.5 = 1.5V$$

Answer: 1.5V

18. In a MOS capacitor with an oxide layer thickness of 10 nm, the maximum depletion layer thickness is 100 nm. The permittivities of the semiconductor and the oxide layer are $\varepsilon_s \; and \; \varepsilon_{OS}$ respectively. Assuming $\varepsilon_s/\varepsilon_{OX} = 3$, the ratio of the maximum capacitance of the minimum capacitance of this MOS capacitor is .

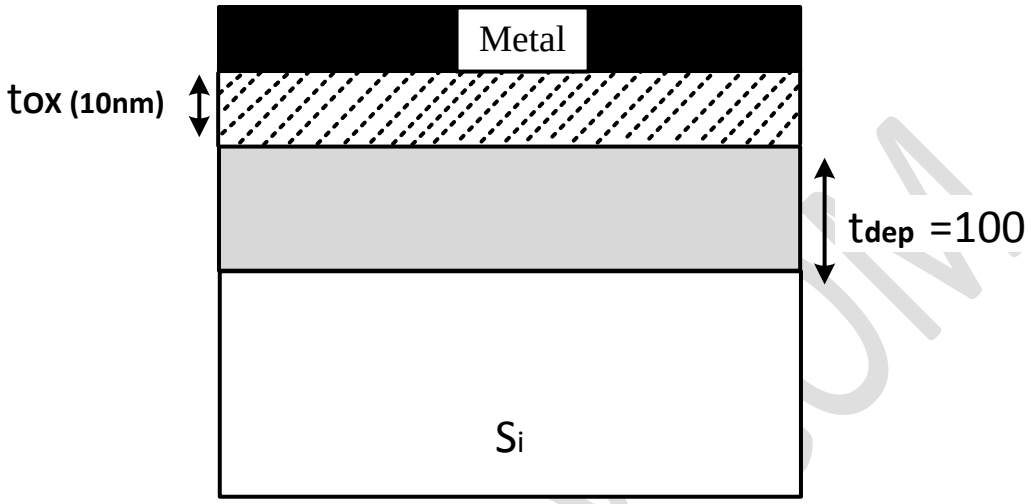
[GATE 2015: 2 Marks]

Soln. Given,

Oxide layer thickness $(t_{OX}) = 10\, nm$

Depletion layer thickness $(t_{dep}) = 100\ nm$

$$\frac{\varepsilon_s}{\varepsilon_{OX}} = 3$$



Both oxide layer capacitance (C_{OX}) and depletion layer capacitances are coming in series, so the maximum capacitance will be when depletion layer capacitance (C_{dep}) will be absent

Maximum capacitance $(C_{max}) = C_{OX}$

Minimum capacitance (C_{min}) is

Given by

$$C_{min} = \frac{C_{OX}\, C_{dep}}{C_{OX} + C_{dep}}$$

Where C_{OX} and C_{dep} are capacitances per unit area

$$\frac{C_{max}}{C_{min}} = \frac{C_{OX}}{\frac{C_{OX}\, C_{dep}}{C_{OX} + C_{dep}}} = \frac{C_{OX} + C_{dep}}{C_{dep}}$$

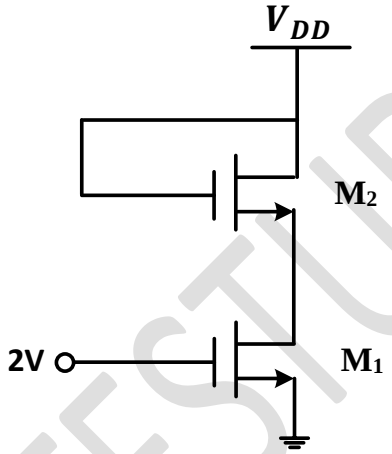
$$= 1 + \frac{C_{OX}}{C_{dep}} = 1 + \frac{\frac{\varepsilon_{OX}}{t_{OX}}}{\frac{\varepsilon_S}{d}}$$

$$= 1 + \frac{\varepsilon_{OX}}{\varepsilon_r} \cdot \frac{d}{t_{OX}}$$

$$\frac{C_{max}}{C_{min}} = 1 + \frac{1}{3} \times \frac{100}{10} = 4.33$$

Answer: 4.33

19. In the circuit shown both enhancement mode NMOS transistor have the following characteristics: $K_n = \mu_n C_{OX}(W/L) = 1mA/V^2; V_{TN} = 1V$. Assume that the channel length modulation parameter λ is zero and body is shorted to source. The minimum supply voltage V_{DD} (in volts) needed to ensure that transistor M_1 operates in saturation mode of operation is __



[GATE 2015: 2 Marks]

Soln. In the given circuit

M_1 is to operate in saturation. Both MOSFETs are NMOS

$$K_n = \mu_n C_{OX}(W/L) = 1\ mA/V^2$$

$$V_{Tn} = 1\ V$$

Both MOSFETs are in series so same current will flow through then

For M_1 : $V_{GS_1} = 2V$ (As per figure)

If M_1 is assumed in saturation, then

$$I_{D_1} = \frac{1}{2} K_n \left[V_{GS_1} - V_T\right]^2$$

Minimum V_{DS} required for M_1 to operate in saturation

$$V_{DS_1} = V_{GS_1} - V_T = 2 - 1 = 1V$$

For M_2 : $V_{GS_2} - V_{DD} - V_{DS_1} = V_{DD} - 1$

$$I_{D_2} = \frac{1}{2} K_n \left[V_{GS_2} - V_T\right]^2$$

Since $I_{D_1} = I_{D_2}$

$$\frac{1}{2} K_n \left[V_{GS_1} - V_T\right]^2 = \frac{1}{2} K_n \left[V_{GS_2} - V_T\right]^2$$

$or,\quad V_{VG_1} - V_T = V_{GS_2} - V_T$

$$V_{GS_1} = V_{GS_2}$$

$or,\quad V_{GS_1} = V_{DD} - 1$

$or,\quad V_{DD} = 2 + 1 = 3V$

Answer: $V_{DD} = 3V$

20. The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain source voltage of 5V. When the drain source voltage was increased to 6V while keeping gate source voltage same. The drain current increased to 1.02 mA. Assume that drain to source saturation voltage is much smaller than the applied drain source voltage. The channel length modulation parameter λ $(in\ V^{-1})$ is _____.

[GATE 2015: 2 Marks]

Soln. Given,

N MOS transistor

Biased in saturation $I_D = 1mA \quad , \quad V_{DS} = 5V$

Drain current in saturation including the effect of channel length modulation parameter

$$I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

So, we can write the ratio of two current

$$\frac{I_{D_2}}{I_{D_2}} = \frac{1 + \lambda V_{DS_2}}{1 + \lambda V_{DS_1}}$$

$$or, \quad \frac{1.02}{1} = \frac{1 + 6\lambda}{1 + 5\lambda}$$

$$or, \quad 1.02 + 5.1\lambda = 1 + 6\lambda$$

$$or, \quad 0.9\,\lambda = 0.02$$

$$or, \quad \lambda = \frac{0.02}{0.9} = 0.022V^{-1}$$

21. Consider an n – channel metal oxide semiconductor field effect transistor (MOSFET) with gate to source voltage of 1.8V. Assume that $\frac{W}{L} = 4, \mu_n C_{OX} = 70 \times 10^{-6}\ AV^{-2}$
The threshold voltage is 0.3V, and the channel length modulation parameter is $0.09V^{-1}$. In the saturation region, the drain conduction (in micro Siemens) is _____

[GATE 2016: 2 Marks]

Soln. Given,

N – MOSFET

$$V_{GS} = 1.8V \ , \ \frac{W}{L} = 4 \ , \ \mu_n C_{OX} = 70 \times 10^{-6}\ AV^{-2}$$

$$V_{TH} = 0.3V \ , \ \lambda = 0.09V^{-1}$$

Drain current in saturation including the effect of channel length modulation is

$$I_D = \frac{1}{2}\,\mu_n\, C_{OX} \left(\frac{W}{L}\right)(V_G - V_T)^2(1 + \lambda V_D)$$

Channel conductance (g_d)

$$(g_d) = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G = constant}$$

$$g_d = \frac{\partial I_D}{\partial V_D} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)(V_G - V_T)^2 \,.\, \lambda$$

So,

$$g_d = \frac{1}{2} \times 70 \times 10^{-6} \times 4 \times (1.8 - 0.3)^2 \times 0.09$$

$$= 140 \times 10^{-6} \times 2.25 \times 0.09$$

$$= 28.35 \times 10^{-6}$$

$$g_d = 28.35\ \mu Siemens$$

Drain conductance $g_d = 28.35\ \mu$ Siemens

22. A voltage V_G is applied across the MOS capacitor with metal Gate and p – type silicon substrate at $T = 300\ K$. The inversion carrier density (in number of units per unit area) for $V_G = 0.8V$ *is* $2 \times 10^{11} cm^{-2}$ *for* $V_G = 1.3V$, the inversion carrier density is $4 \times 10^{11} cm^{-2}$. What is value of inversion carrier density of V_G = 1.8V

(a) $4.5 \times 10^{11} cm^{-2}$ (c) $7.2 \times 10^{11} cm^{-2}$

(b) $6.0 \times 10^{11} cm^{-2}$ (d) $8.4 \times 10^{11} cm^{-2}$

[GATE 2016: 2 Marks]

Soln. Given,

For V_G = 0.8V

Inversion layer carrier density $= 2 \times 10^{11} cm^{-2}$

For $V_G = 1.3V$, ***Inversion layer carrier density*** $= 4 \times 10^{11} cm^2$

Find for V_G = 1.8 V

For MOS capacitor

Charge $(Q) \propto (V_G - V_T)$

Charge $Q_1 = K.(V_G - V_T)$

Or, $Q_1 = qA \times inversion\ carrier\ density$

So,

$$\frac{2 \times 10^{11} \,.\, qA}{4 \times 10^{11} \,.\, qA} = \frac{(0.8 - V_T)}{(1.3 - V_T)}$$

Or, $V_T = 0.3V$

$Now\ for\ V_G = 1.8V \ ,\ Q_1 = qA\,\rho_i$

Where ρ_i is inversion carrier density

$$\frac{\rho_i\, q \,.\, A}{2 \times 10^{11}\, q \,.\, A} = \frac{(1.8 - 0.3)}{(0.8 - 0.3)}$$

$or,\ \rho_i = 6 \times 10^{11}/cm^2$

Option (b)

23. Consider long channel N MOS transistor with source and body connected together.
Assume that the electron mobility is dependent of V_{GS} and $V_{DS.}$ Given,
$g_m = 0.5\,\mu A/V \ for\ V_{DS} = 50\ mV\ and\ V_{GS} = 2V$
$g_d = 8\,\mu A/V \ for\ V_{GS} = 2V\ and\ V_{DS} = 0V$
Where
$g_m = \frac{\partial\, I_D}{\partial\, V_{GS}}\ and\ g_d = \frac{\partial\, I_D}{\partial\, V_{DS}}$
The threshold voltage (in volts) of the transistor is _____

[GATE 2016: 2 Marks]

Soln. Given long channel N MOS, it means it does not have the effect of channel length modulation. Since V_{DS} is 50 mV (small) it is operating in linear region. The drain current is given by

$$I_D = \mu_n\, C_{OX} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$g_m = \frac{\partial\, I_D}{\partial\, V_{GS}} = \mu_n\, C_{OX} \left(\frac{W}{L}\right) .V_{DS}$$

$$or, \quad \mu_n C_{OX} \frac{W}{L} = \frac{g_m}{V_{DS}} = \frac{0.5 \times 10^{-6}}{50 \times 10^{-3}} = 10 \times 10^{-6}$$

Now,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{OX} \frac{W}{L} [V_G - V_T]$$

$$or, \quad 8 \times 10^{-6} = 10 \times 10^{-6} [V_{GS} - V_T]$$

$$or, \quad V_{GS} - V_T = \frac{8 \times 10^{-6}}{10 \times 10^{-6}}$$

$$or, \quad V_T = V_{GS} - 0.8$$

$$= 2 - 0.8 = 1.2V$$

$$\textbf{Answer: } V_T = 1.2V$$

24. Figure I and II show two MOS capacitors of unit area. The capacitor in Figure I has insulator material X of (thickness t_1 = 1 nm and dielectric constant $\in_1 = 4$) and y (of thickness $t_2 = 3nm$ and dielectric constant$\in_1 = 20$). The capacitor in figure II has only insulator material X of thickness t_{eq} . If the capacitors are of equal capacitance, then the value of t_{eq} (in nm) is_____

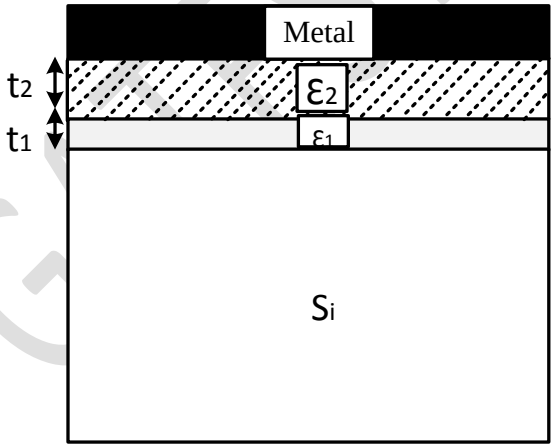


Figure I

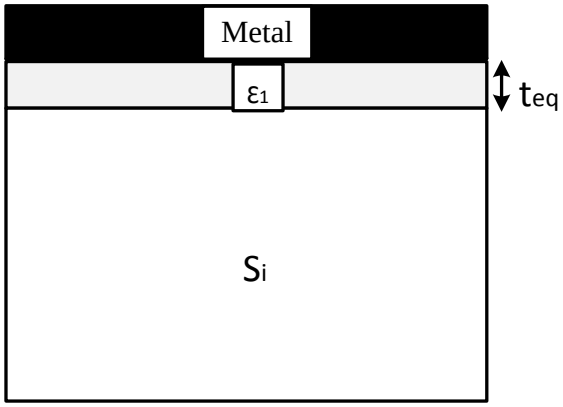


Figure II

[GATE 2016: 2 Marks]

Soln. MOS structure is like a parallel plate capacitor

The capacitance per unit area for this geometry is

$$C' = \frac{\in}{d}$$

Where $\in$ is permittivity of insulator

d is distance between plates

For area A,

$$C = \frac{\in A}{d}$$

As per figure I the two capacitors formed by the two dielectrics are in series

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

$$= \left[\frac{\frac{4}{1\times10^{-9}} \times \frac{20}{3\times10^{-9}}}{\frac{4}{1\times10^{-9}} + \frac{20}{3\times10^{-9}}}\right] \in_0$$

$$C = 2.5 \times 10^9 \ \in_0$$

For the II case

$$C = \frac{\in_r \in_0}{t_{eq}}$$

$$or, \quad t_{eq} = \frac{\in_r \in_0}{C}$$

$$= \frac{\in_r \in_0}{2.5\times10^9 \ \in_0} = \frac{4}{2.5\times10^9}$$

$$= 1.6 \times 10^{-9}\ m$$

$$t_{eq} = 1.6\ nm$$

Ans.1.6 nm